# SY50355

## CCM + QR Flyback Converter with E-Mode GaN Integrated

## General Description

The SY50355 is a high frequency flyback converter operating in continuous conduction mode (CCM) and quasi-resonant (QR) mode. It integrates an enhancement-mode (E-Mode) GaN FET to enable a compact PCB layout. The device is designed for power delivery (PD) capable adapters and quick chargers. Its maximum operating frequency of up to 500kHz allows for reduced transformer, PCB, and capacitor sizes.

The SY50355 operates using peak current control. At low input voltage and heavy load the device enables CCM mode, allowing for reduced transformer and PCB size. At high input voltage, CCM mode is disabled, and the SY50355 switches to QR mode. In this mode, the GaN FET turns on at the valley point to minimize switching losses. As the load decreases, the SY50355 enters DCM mode to lower the switching frequency and improve efficiency. Under very light load conditions, the device enters burst mode to further reduce power loss.

The SY50355 integrates comprehensive protection features to ensure reliable operation, including high voltage (HV) startup, brown-out protection, output and VCC overvoltage protection (OVP), output undervoltage protection (UVP), internal and external overtemperature protection (OTP), and open-loop protection (OLP).

It is recommended to use the SY5236 or SY5236A as a secondary-side synchronous rectifier (SR) controller in conjunction with the SY50355 to enable zero voltage switching (ZVS) at high input voltage for improved efficiency.

The SY50355 is available in a compact SSOP9E package.

## Features

- Integrated 700V E-Mode GaN FET (160mΩ)
- Combined CCM+QR Operating Modes
- Soft GaN Gate Drive for Optimized EMI Performance
- Wide VCC Operating Range: 7-85V
- Switching Frequency Range: 25kHz–500kHz
- Frequency Modulation to Reduce EMI Noise
- Integrated 700V HV Startup Circuitry
- Programmable Output OVP and UVP
- Brown-In/Out Protection
- Current Sense Resistor Short-Circuit Protection
- Winding or SR Short-Circuit Protection
- Internal and External OTP
- Compact Package: SSOP9E

## Applications

- AC/DC Adapters
- PD Adapters
- Quick Chargers

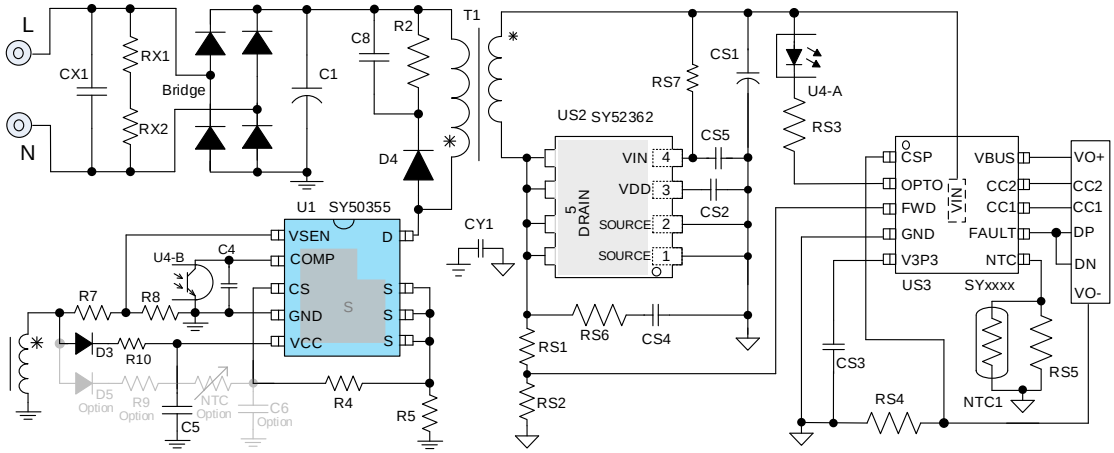


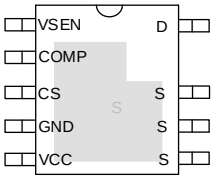

*Figure 1. Typical Application Using Synchronous Rectification (SR)*

## Ordering Information

| Ordering Part Number | Package type | Top Mark |
|---|---|---|
| SY50355HZP | SSOP9E RoHS-Compliant and Halogen-Free | **ABBLxyz** |

***x = year code, y = week code, z = lot number code***

## Pinout (top view)




## Pin Description

| Pin No | Pin Name | Pin Description |
|---|---|---|
| 1 | VSEN | Output voltage, input voltage, and QR valley detection pin. |
| 2 | COMP | Secondary side compensation voltage, connected to an optocoupler. |
| 3 | CS | Current sensing pin, external OTP pin. |
| 4 | GND | Ground pin. |
| 5 | VCC | Power supply pin. |
| 6, 7, 8 | S | Source of integrated GaN. |
| 9 | D | HV startup, drain of integrated GaN. |
| Bottom PAD | S | Source of integrated GaN. |

## Block Diagram

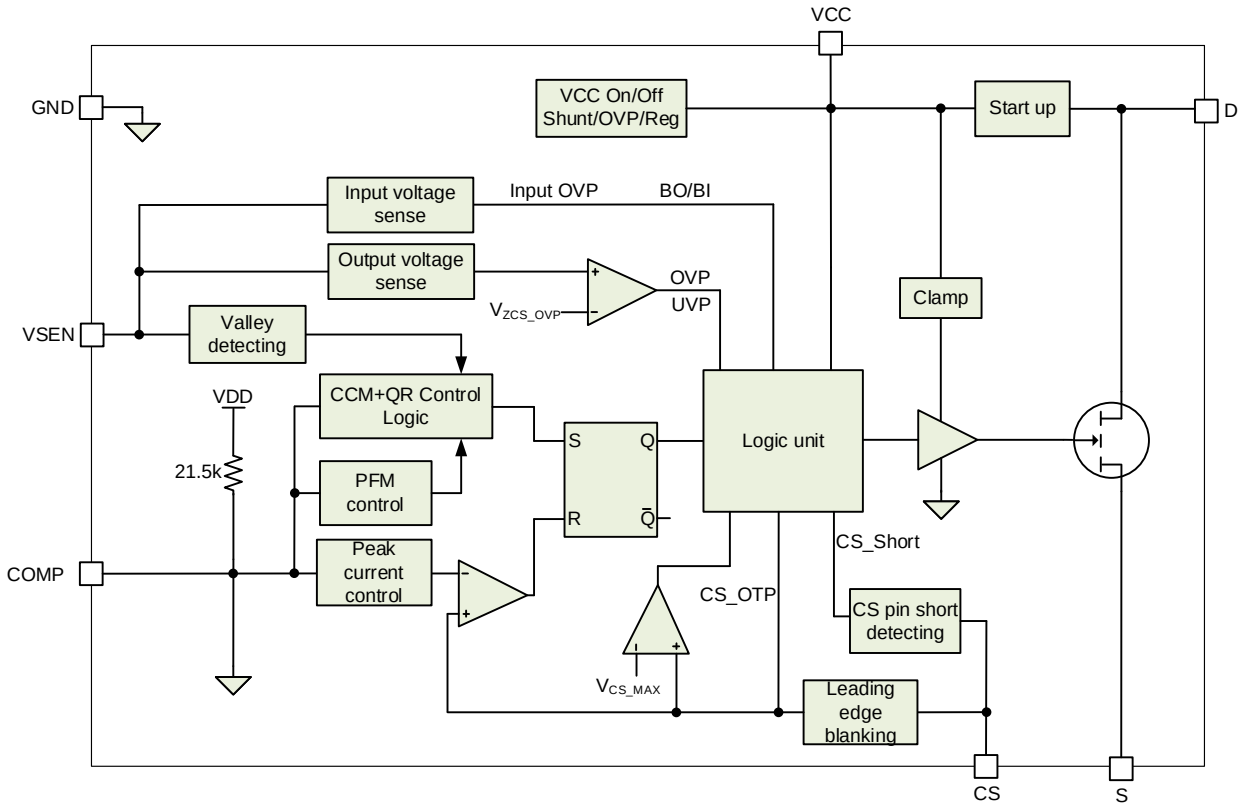



*Figure 2. Block Diagram*

## Absolute Maximum Ratings

| Parameter (Note 1) | Min | Max | Unit |
|---|---|---|---|
| D (Drain source voltage) | -0.3 | 700 | V |
| D Pulsed Voltage (Intended for a repetitive pulse, TPULSE < 100 ns) | -0.3 | 750 | |
| VCC | -0.3 | 100 | |
| CS, COMP | -0.3 | 4 | |
| VSEN | -1 (Note 1) | 7 | |
| Junction Temperature, Operating | -40 | 150 | °C |
| Lead Temperature (Soldering, 10s) | | 260 | |
| Storage Temperature Range | -60 | 150 | |
| Dynamic VSEN Negative Voltage in 50μs Duration (Note 1) | | -1 | V |
| Dynamic VSEN Negative Current in 50μs Duration (Note 1) | | -2 | mA |
| Human Body Model ESD (HV Pin and VCC Pin) per ESDA/JEDEC JS-001-2017 (Note 6) | | ±1 | kV |
| Human Body Model ESD (All Pins Except HV Pin and VCC Pin) per ESDA/JEDEC JS-001-2017 (Note 6) | | ±2 | kV |
| Charged Device Model ESD per JS-002-2018 (Note 6) | | ±500 | V |
| Latch-Up Test per JEDEC78E (Note 6) | | ±100 | mA |
| MSL Rating | | 3 | |

## Thermal Information

| Parameter (Note 2) | Min | Max | Unit |
|---|---|---|---|
| $\theta_{JA}$ Junction-to-Ambient Thermal Resistance | | 123.5 | °C/W |
| $\theta_{JC}$ Junction-to-Case Thermal Resistance | | 46 | |
| PD Power Dissipation TA = 25°C | | 1.01 | W |

## Recommended Operating Conditions

| Parameter (Note 3) | Min | Max | Unit |
|---|---|---|---|
| D (Drain) | -0.3 | 700 | V |
| VCC | 7 | 85 | |
| CS | -0.3 | 0.6 | |
| VSEN | -0.3 | 3.0 | |
| COMP | -0.3 | 3.0 | |
| Junction Temperature Range | -40 | 125 | °C |
| Case Temperature Range | -40 | 105 | °C |

## Electrical Characteristics

($V_{VCC}$ = 13V (Note 7), $T_J$ = 25°C unless otherwise specified (Note 4))

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| D (Drain) (HV) | Drain Source Voltage | $V_{DS\_MAX}$ | VGS=0V, ID<30μA | 700 | | | V |
| | Turn On Resistance | $R_{DS\_ON}$ | VGS=6V | | 160 | 210 | mΩ |
| | Leakage Current | $I_{HV\_LK}$ | $V_{HV}$ =700$V_{DC}$ | | | 30 | μA |
| | HV Charge VCC | $I_{HV\_CHARGE}$ | $V_{HV}$ = 100$V_{DC}$ | 1.60 | 2.15 | 2.70 | mA |
| VCC | Start-up Current | $I_{CC\_START}$ | $V_{CC}$=$V_{CC,ON}$-0.5V | 30 | 42 | 55 | μA |
| | Turn-On Threshold | $V_{CC\_ON}$ | $V_{CC}$ rising up | 16.0 | 17.5 | 19.0 | V |
| | Turn-Off Threshold | $V_{CC\_OFF}$ | $V_{CC}$ falling down | 5.3 | 5.8 | 6.3 | V |
| | Regulation Threshold | $V_{CC\_REG}$ | In error mode | 5.7 | 6.1 | 6.5 | V |
| | OVP Threshold | $V_{CC\_OVP}$ | | 86 | 92 | 98 | V |
| | OVP Debounce Cycles | $N_{VCCOVP\_DBC}$ | (Note 8) | | 4 | | cycles |
| | Current Sink at OVP | $I_{CC\_SHUNT}$ | $V_{CC}$=$V_{CC\_OVP}$+1V | 2.4 | 3.0 | 3.6 | mA |
| | Operating Current | $I_{CC\_OPERATING}$ | | | 0.6 | | mA |
| | VCC Current in Burst | $I_{CC\_BURST}$ | $V_{COMP}$<0.27V | 130 | 160 | 190 | μA |
| CS | Maximum Peak Current | $V_{CS\_MAX}$ | | 550 | 600 | 650 | mV |
| | Leading Edge Blanking Time for $V_{CS\_MAX}$ | $t_{CS\text{-}LEB1}$ | | | 100 | | ns |
| | Debounce of $V_{CS\_MAX}$ | $N_{VCSMAX\_DBC}$ | (Note 8) | | 4 | | cycles |
| | Vcs Limitation | $V_{CS\_LIMIT}$ | | 373 | 395 | 417 | mV |
| | Leading Edge Blanking Time for $V_{CS\_LIMIT}$ | $t_{CS\_LEB3}$ | | 180 | 280 | 380 | ns |
| | Current Mirror in ton | $K_{VSEN\text{-}CS}$ | $I_{VSEN}$/ $I_{CS}$ | | 20:1 | | / |
| | Detection of CS short | $t_{CS\_SHORT}$ | Only in soft-start | 4.0 | 5.8 | 7.6 | μs |
| | Threshold for CS short | $V_{CS\_SHORT}$ | | 45 | 65 | 85 | mV |
| | Vcs Modulation | $K_{VCS\_MOD}$ | (Note 8) | | ±5% | | / |
| | Frequency Modulation. | $F_{MODULATION}$ | | | 4 | | kHz |
| | Debounce of CS_OTP | $N_{CSOTP}$ | (Note 8) | | 4 | | cycles |
| | Soft Start Time | $t_{SS}$ | (Note 8) | | 7 | | ms |
| VSEN | Output OVP Threshold | $V_{VSEN\_OVP}$ | | 2.03 | 2.14 | 2.25 | V |
| | Blanking Time | $t_{VSEN\_BLK}$ | | 1.2 | 1.5 | 1.75 | μs |
| | Debounce of OVP | $N_{VSEN\_OVP}$ | (Note 8) | | 4 | | cycles |
| | Output UVP Threshold | $V_{VSEN\_UVP}$ | After soft-start | 125 | 150 | 175 | mV |
| | Debounce of UVP | $N_{VSEN\_UVP}$ | | | 4 | | cycles |
| | BO Threshold Current | $I_{VSEN\_BO}$ | | 90 | 100 | 110 | μA |
| | BO Debounce Time | $t_{BO\_DBC}$ | | | 150 | | ms |
| | Restart Time 1 | $t_{ERROR\_SHORT}$ | Short error mode | | 0.3 | | s |
| | Restart Time 2 | $t_{ERROR}$ | Error mode | | 2.0 | | s |
| | BI Threshold Current | $I_{VSEN\_BI}$ | | 104 | 118 | 132 | μA |
| | AC high Line Threshold | $I_{VSEN\_ACHIGH}$ | | 205 | 225 | 245 | μA |

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| | Back to AC Low Line | $t_{ACLOW\_DBC}$ | Debounce time | | 60 | | ms |
| | Timeout when Valley Cannot be Detected | $t_{TIMEOUT}$ | | | 10 | | µs |
| | Valley Point Threshold | $V_{VSEN\_VALLEY}$ | | | 0 | | mV |
| | Turn on Delay in QR | $t_{VSEN\_DELAY}$ | | | 150 | | ns |
| COMP | Internal Pull up Voltage | $V_{COMP\_UP}$ | | 2.3 | 2.8 | 3.3 | V |
| | Internal Pull up Resistor | $R_{COMP\_PU}$ | | 16.0 | 21.5 | 27.0 | kΩ |
| | OLP Threshold | $V_{COMP\_OLP}$ | $V_{COMP}$ >$V_{COMP\_OLP}$ | 2.2 | 2.5 | 2.8 | V |
| | OLP Debounce Time | $t_{OLP\_DBC}$ | | 110 | 150 | 190 | ms |
| | DCM to QR Threshold | $V_{COMP\_DCMQR}$ | | | 0.935 | | V |
| | QR to DCM Threshold | $V_{COMP\_QRDCM}$ | | | 0.915 | | V |
| | Sleep in Threshold | $V_{COMP\_SLEEPIN}$ | $V_{COMP}$ fall down | 0.24 | 0.27 | 0.30 | V |
| | Sleep out Threshold | $V_{COMP\_SLEEPOUT}$ | $V_{COMP}$ rising up | 0.29 | 0.325 | 0.36 | V |
| Switching Frequency | Maximum Fsw in CCM | $F_{SW\_MAXCCM}$ | | 77 | 85 | 93 | kHz |
| | Maximum Fsw in DCM | $F_{SW\_MAXDCM}$ | | | 50 | | kHz |
| | Minimum Fsw in DCM | $F_{SW\_MINDCM}$ | $V_{COMP}$=0.25V | 20 | 24 | 28 | kHz |
| | Maximum ON Time | $t_{ON\_MAX}$ | | 14 | 20 | 26 | µs |
| | Maximum Off Time | $t_{OFF\_MAX}$ | | 100 | 140 | 180 | µs |
| Internal OTP | OTP Threshold | $T_{OTP\_SHUNTDOWN}$ | (Note 5) | | 150 | | °C |
| | Recovery Threshold | $T_{OTP\_RECOVERY}$ | (Note 5) | | 130 | | °C |

**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:** $\theta_{JA}$ is measured with natural convection at $T_A$ = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standards. Test conditions: Device mounted on “2 x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal via to bottom layer ground plane.

**Note 3:** The device is not guaranteed to function outside its operating conditions.

**Note 4:** Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25°C. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

**Note 5:** Guaranteed by design or statistical correlation and not production tested.

**Note 6:** Meets ESDA/JEDEC JS-001-2017 and JEDEC78E.

**Note 7:** Increase VCC pin voltage gradually higher than the $V_{CC\_ON}$ voltage, then reduce it to 13V.

**Note 8:** Application test result.

# Detailed Description

### HV (D Pin) Startup and Power Supply

At power-on, the D pin charges the VCC capacitor. When VCC voltage rises above the startup threshold, the HV circuitry will be turned off to reduce power loss.

If the device enters protection mode, PWM operation is suspended for a fixed error timeout period ($t_{ERROR}$). During this time, internal power consumption causes the VCC voltage to drop. When VCC falls below the regulation threshold ($V_{CC\_REG}$) the HV circuitry is reenabled to recharge the capacitors until VCC > $V_{CC\_ON}$. After $t_{ERROR}$, the internal logic will be reset, and a restart sequence is initiated.

### Input Voltage Detection

The SY50355 monitors the input voltage through the VSEN pin during the $t_{ON}$ period (when the GaN FET is on). During $t_{ON}$, the VSEN pin is clamped to approximately 0V. If the current at the VSEN pin is higher than $I_{VSEN\_ACHIGH}$, an AC high condition is immediately assumed. If the current remains below $I_{VSEN\_ACHIGH}$ for a duration longer than $t_{ACLOW\_DBC}$, an AC low condition is assumed.

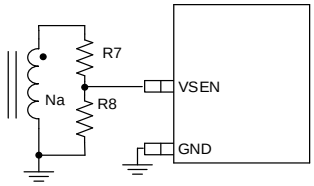



*Figure 3. Input Voltage Detection*

During the $t_{ON}$ period, a current flows from the VSEN pin to Na through resistor R7. The AC high threshold can be calculated as follows:

$$V_{BUS\_ACHIGH} = I_{VSEN\_ACHIGH} \times R7 \times \frac{Np}{Na}$$

(Na is auxiliary winding. Np is primary winding.)

### Valley Detection

The following waveform illustration shows the valley detection method. When the falling edge of the zero-crossing voltage is detected at the VSEN pin, the SY50355 will turn on the GaN FET after a fixed delay.

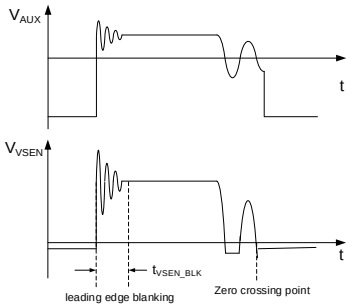



*Figure 4. Valley Detection*

Noise is present at the VSEN pin when the GaN FET turns off, which may affect valley detection. The SY50355 uses a $t_{VSEN,\ BLK}$ time to avoid noise interference.

### CCM Mode

When the input voltage is detected as AC low, CCM operation is allowed. In this condition, the valley count is reduced to the first valley. As the load continues to go up, the switching frequency decreases. If no valley signal is detected before the internal frequency clock expires, the PWM turns on at the clock edge, and CCM operation is automatically enabled.

### QR Mode

When the input voltage is detected as AC high, CCM operation is disabled. In QR mode, the PWM turns on at the valley point of the GaN FET drain voltage, improving both EMI performance and efficiency. The peak current threshold ($V_{CSPK}$) is controlled by the compensation voltage ($V_{COMP}$). When $V_{COMP}$ is higher than $V_{COMP\_DCMQR}$, QR mode is enabled starting with the 6$^{th}$ valley number. As the load increases, the valley number decreases in one-step increments until it reaches the first valley.

### DCM Mode

When $V_{COMP}$ is lower than $V_{COMP\_QRDCM}$, DCM mode is enabled. In DCM mode, $V_{CSPK}$ and the switching frequency are controlled by $V_{COMP}$. PWM turns on instantly at the $F_{SW}$ clock and does not wait for the valley point. As the load decreases, frequency and $V_{CSPK}$ decrease to keep a constant output voltage.

### Burst Mode

When both the switching frequency and $V_{CSPK}$ have decreased to respective minimum values, if the output load continues decreasing, $V_{COMP}$ will be lower than $V_{COMP\_SLEEPIN}$. At this point, PWM operation will stop. PWM resumes only when $V_{COMP}$ rises above the $V_{COMP\_SLEEPOUT}$ threshold. In this condition, the device operates in burst mode.

### Soft-Start

At startup, when $V_{COMP}$ rises above the $V_{COMP\_SLEEPOUT}$ threshold, PWM operation begins, and the current sense threshold ($V_{CS}$) increases step by step from the minimum value across seven steps. Under heavy load or $V_{OUT}$ short conditions, the soft-start period terminates after $t_{SS}$. Under light load or no-load conditions, if the $V_{CS}$ value determined by $V_{COMP}$ is lower than the value determined by soft-start, the soft-start sequence will terminate and $V_{COMP}$ takes control of $V_{CS}$.

#### $V_{CS\_LIMIT}$

After $t_{CS\_LEB3}$ in each switching cycle, if $V_{CS}$ is higher than the $V_{CS\_LIMIT}$, PWM turns off immediately. This decision is

made on a cycle-by-cycle basis and does not affect the PWM operation of the subsequent cycle.

### $V_{CS\_MAX}$ Protection during Transformer Winding Short Circuit

Under normal operating conditions, $V_{CS\_LIMIT}$ restricts the GaN peak current to ensure sufficient protection. However, in the event of a transformer winding or secondary diode short circuit, the current slope becomes extremely steep, causing the transformer to enter saturation state. As a result, the current can rise to a much higher level during $t_{CS\_LEB3}$.

To address this, the SY50355 monitors $V_{CS}$ after $t_{CS\_LEB1}$, which is shorter than $t_{CS\_LEB3}$. If $V_{CS}$ is higher than $V_{CS\_MAX}$ for four consecutive cycles, PWM operation stops and the timer starts. After the $t_{ERROR}$ period, the internal logic resets, and a restart is triggered, with the HV circuitry recharging VCC to the $V_{CC\_ON}$ threshold.

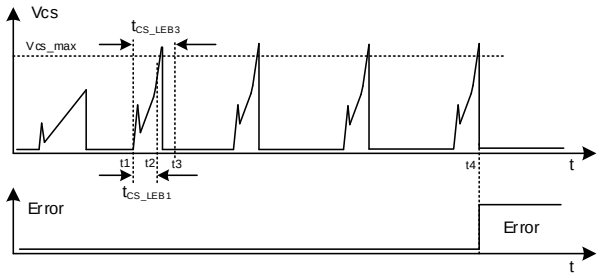



*Figure 5. $V_{CS\_MAX}$ Process*

### Brown-In and Brown-Out

When the input voltage falls below 90VAC, the current and heat dissipation in the transformer and primary GaN FET increase significantly. To protect the power supply, the SY50355 provides brown-in (BI) and brown-out (BO) protections using the VSEN pin.

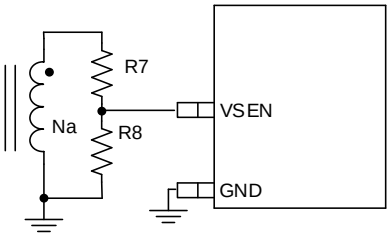



*Figure 6. Brown out Detection*

During the $t_{ON}$ period, the VSEN pin is clamped to approximately 0V. A current flows from the VSEN pin to Na through resistor R7. Brown-in and brown-out are defined as follows:

- Brown-In (BI): During $t_{ON}$, if the VSEN current is higher than $I_{VSEN\_BI}$ a brown-in condition is confirmed.
- Brown-Out (BO): During $t_{ON}$, if the VSEN current is lower than $I_{VSEN\_BO}$ for a duration longer than $t_{BO\_DBC}$ a brown-out condition is triggered.

The BO threshold is determined by R7, with the bus voltage at brown-out calculated as:

$$V_{BUS\_BO} = I_{VSEN\_BO} \times R7 \times \frac{Np}{Na}$$

(Na is auxiliary winding. Np is primary winding.)

Following a BO event, PWM operation stops. After a $t_{ERROR\_SHORT}$ delay, the internal logic resets and a startup sequence is initiated, with the HV input recharging VCC to the $V_{CC\_ON}$ threshold. After restart, one PWM pulse is generated, and the VSEN pin current will be detected. If the BI condition is met, PWM operation continues and the SY50355 will recover to normal operating state.

### Output OVP and UVP

The SY50355 detects the output voltage through the VSEN pin and provides output overvoltage protection (OVP) and undervoltage protection (UVP).

When VSEN voltage is higher than $V_{VSEN\_OVP}$ for $N_{VSEN\_OVP}$ cycles, $V_{SEN\_OVP}$ is triggered and PWM stops. After a $t_{ERROR}$ delay, the logic will be reset and a startup sequence is initiated, with the HV circuitry charging VCC to $V_{CC\_ON}$.

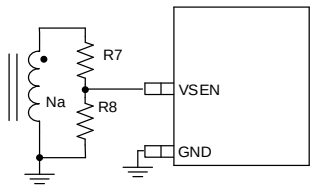



*Figure 7. VSEN OVP and UVP Setting*

The output OVP threshold is calculated as follows:

$$V_{OUT\_OVP} = V_{VSEN\_OVP} \times \frac{R7 + R8}{R8} \times \frac{Ns}{Na}$$

(Na is auxiliary winding. Ns is secondary winding.)

After the soft-start time, when VSEN voltage is lower than $V_{VSEN\_UVP}$ continuously for $N_{VSEN\_UVP}$ cycles, $V_{SEN\_UVP}$ is triggered and PWM stops. After a $t_{ERROR}$ delay, the logic will be reset and a startup sequence is initiated, with the HV circuitry charging VCC to $V_{CC\_ON}$.

R7 is determined by the brown-out threshold. R8 is determined by the output OVP threshold. UVP is used to avoid continuous operation under $V_{OUT}$ short circuit conditions and is not mandatory for the design.

### VCC OVP

The SY50355 provides VCC overvoltage protection (OVP) to protect the device from abnormal high voltage caused by an open feedback loop or improper $N_A$ winding turns. When VCC rises to $V_{CC\_OVP}$ and external power current capability is higher than the shunt ability, VCC can continue rising.

VCC is continuously monitored. If VCC is higher than $V_{CC\_OVP}$ for $N_{VCCOVP\_DBC}$ cycles, $V_{CC\_OVP}$ is triggered and PWM stops. After a $t_{ERROR}$ delay, the logic will be reset and a startup sequence is initiated, with the HV circuitry charging VCC to $V_{CC\_ON}$.

**Open-Loop Protection**

If the output is short-circuited or the load increases excessively, the optocoupler circuitry opens and $V_{COMP}$ increases. When $V_{COMP}$ exceeds $V_{COMP\_OLP}$ and remains above this threshold for $t_{OLP\_DBC}$, open-loop protection (OLP) is triggered and PWM stops. After a $t_{ERROR}$ delay, the logic will be reset and a startup sequence is initiated, with the HV circuitry charging VCC to $V_{CC\_ON}$.

**CS Pin Short Circuitry**

During soft-start, $V_{CS}$ is sampled at $t_{CS\_SHORT}$ during the $t_{ON}$ period of every PWM cycle and compared with $V_{CS\_SHORT}$. If $V_{CS} < V_{CS\ SHORT}$ continuously for 2 cycles, short-circuit protection is triggered and PWM stops. After a $t_{ERROR}$ delay, the logic will be reset and a startup sequence is initiated, with the HV circuitry charging VCC to $V_{CC\_ON}$.

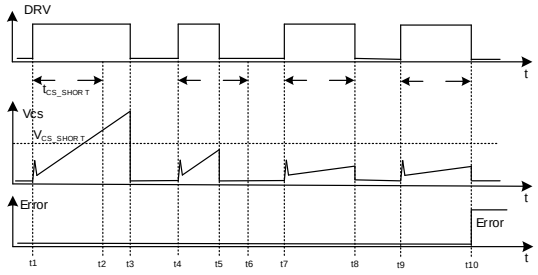



*Figure 8. CS Short Protection*

Figure 8 shows the short protection logic:

- At t2, $V_{CS}$ is higher than $V_{CS\_SHORT}$. No protection.
- At t5, the $t_{CS\ SHORT}$ timer has not expired. No comparison is needed. No protection.
- At t8, $V_{CS}$ is lower than $V_{CS\_SHORT}$ at $t_{CS\ SHORT}$ mark. This is the first cycle.
- At t10, $V_{CS}$ short circuitry has been detected in 2 consecutive cycles, protection is triggered.

**Internal OTP**

The SY50355 continuously monitors the die temperature during normal operation. When the die temperature rises above $T_{OTP,\ SHUTDOWN}$, PWM operation stops. After a $t_{ERROR}$ delay, the logic resets, and a startup sequence is initiated, with the HV circuitry charging VCC to $V_{CC\_ON}$. After restart, PWM resumes normal operation once the temperature falls down below $T_{OTP,\ RECOVERY}$.

# Design Guide

**BUS Capacitor Selection**

The bulk capacitor $C_{BUS}$ is generally selected according to the following guidelines (PFC refers to Power Factor Correction):

- Without PFC: 1.0–1.5μF per watt of output power.
- With PFC: 0.5–1.0μF per watt of output power.

**Minimum BUS Voltage**

The minimum BUS voltage occurs when the input voltage $V_{AC}$ is at its lowest and the output current reaches its maximum rated value. Calculating the required BUS capacitance involves assumptions and estimated parameters, which often lead to inaccurate results, which often lead to inaccurate results. Additionally, the actual capacitance of aluminum capacitors is only 85-90% of the nominal value, further reducing calculation accuracy. Therefore, precise results are difficult to obtain through calculation alone.

The following examples are helpful for fast selection and can be used as a reference.

For a 30~45W solution without PFC (Power Factor Correction) circuitry, a bus capacitor configuration of 27μF + 27μF is recommended. The corresponding $V_{BUS\_MIN}$ is as follows:

| Output Power | 30W | 35W | 40W | 45W |
|---|---|---|---|---|
| AC90V 50Hz | 86V | 80V | 75V | 68V |
| AC90V 60Hz | 93V | 87V | 83V | 78V |

For a 66W solution without PFC circuitry, operating under full load conditions (20V, 3.3A) the corresponding $V_{BUS\_MIN}$ is as follows:

| Bus Nominal Capacitance | 82+22μF | 82+10μF | 82μF | 68μF |
|---|---|---|---|---|
| AC90V 50Hz | 82V | 78V | 72V | 60V |

For a 140W solution using a boost PFC plus flyback topology, the output is 28V at 5A. The bus nominal capacitance is 39 μF + 39 μF.

● At AC 90V, 50Hz, the boost PFC outputs DC 240V. $V_{BUS}$ ranges from 222V (min) to 253V (max), resulting in a ripple of 31V.

● At AC 176V, 50Hz, boost PFC outputs DC 350V. $V_{BUS}$ ranges from 338V (min) to 362V (max), resulting in a ripple of 24V.

For optimal performance, $V_{BUS\_MIN}$ should be higher than DC 60V.

**Transformer Calculation (CCM, AC90-264V without PFC)**

**(1) Primary/secondary turns ratio: $N_{PS}$**

$N_{PS}$ can be calculated by the following formula:

$$V_{OR} = N_{PS} \times (V_O + V_{D\_F})$$

$V_{OR}$ is the reflected voltage on the primary winding. A typical value ranges from 80~130V. $V_O$ is the output voltage. $V_{D\_F}$ is the forward voltage of the secondary rectification diode. If a synchronous rectified (SR) is used on the secondary side, set $V_{D\_F}$ = 0.

**(2) Select transformer ($A_e$ and Bobbin)**

The transformer should be selected based on output power, enclosure size, and BOM cost. The following examples provide useful references for quick selection:

- 65W, ATQ18, $A_e$ = 62mm², winding width = 6.0mm
- 80W, PQ22.5, $A_e$ = 73mm², winding width = 9.5mm
- 100W, ATQ24, $A_e$ = 90mm², winding width = 8.0mm
- 140W, RM10, $A_e$ = 98mm², winding width = 10.3mm

The winding width of the bobbin is a critical parameter. A wider winding area reduces leakage inductance and allows for thicker winding wires, which improves efficiency.

**(3) Select $N_S$ wire diameter and turns**

To meet safety standards, the secondary (Ns) winding should use triple-insulated wire. The diameter of the triple-insulated wire is determined by the output current. The following examples are helpful for quick selection:

- 20V 3.3A, ATQ18, width=6.0mm, 0.10*80mm*1, Ns=4ts.
- 11V 7.3A, PQ22.5, width=9.5mm, 0.10*60mm*2, Ns=4ts.
- 20V 5A, ATQ24, width=8.0mm, 0.10*100mm*1, Ns=5ts.
- 28V 5A, RM10, width=10.3mm, 0.10*120mm*1, Ns=6ts.

**(4) Calculate transformer ($N_P$):**

$$N_P = N_{PS} * N_S$$

**(5) Calculate primary inductance) ($L_P$):**

$$L_P = \frac{N_{PS}*V_{BUS_{MIN}}}{I_{OUT_{OLP}}*(V_{OR}+V_{BUS_{MIN}})} * \left( B_{MAX} * A_e * N_P - \frac{V_{OR}*V_{BUS_{MIN}}*T_{SW}}{2*(V_{OR}+V_{BUS_{MIN}})} \right)$$

Where:

- $I_{OUT\_OLP}$ is the output overload protection threshold (unit: A).
- $B_{MAX}$ is B of the transformer (typically 0.35~0.37T; unit: T).
- $T_{SW}$ is the switching period in CCM, calculated as $1000/F_{SW,MAXCCM}$ (unit: μs).

**(6) Calculate current sense resistor ($R_{CS}$):**

$$R_{CS} = \frac{L_P * V_{CS\_LIMIT}}{B_{MAX} * A_E * N_P}$$

Where:

- $V_{CS\_LIMIT}$ is the Vcs limitation value as specified in the EC table.

In the $L_P$ calculation, $N_S$ and $N_P$ are determined first. This method eliminates the need for iterative adjustments and consistently results in a satisfactory design, achieving efficiency that is close to optimal for a given transformer.

**Transformer Calculation (QR, AC176-264V or With PFC)**

**(1) Primary-to-secondary turns ratio ($N_{PS}$):**

Same as in the *CCM, AC 90-264V and No PFC* section.

**(2) Select transformer (Ae and Bobbin):**

Same as in the *CCM, AC90-264V and No PFC* section.

**(3) Select $N_S$ wire gauge and turns:**

Same as in the *CCM, AC90-264V and No PFC* section.

**(4) Calculate transformer ($N_P$):**

Same as in the *CCM, AC90-264V and No PFC* section.

**(5) Calculate Primary Inductance ($L_P$):**

$$L_P = \frac{B_{MAX} * A_E * N_{PS} * N_P * V_{BUS_{MIN}}}{2 * I_{OUT_{OLP}} * (V_{OR} + V_{BUS_{MIN}})}$$

- $B_{MAX}$ is B of the transformer (typically 0.35~0.37T; unit: T)
- $I_{OUT\_OLP}$ is the output overload protection threshold (unit: A).

**(6) Calculate current sense resistor ($R_{CS}$):**

$$R_{CS} = \frac{V_{CS\_LIMIT} * N_{PS} * V_{BUS\_MIN}}{2 * I_{OUT_{OLP}} * (V_{OR} + V_{BUS\_MIN})}$$

Where:

- $V_{CS\_LIMIT}$ is the Vcs limitation value as specified in the EC table.

**Turns of auxiliary winding: $N_A$**

At $V_{OUT\_MIN}$, AUX winding should supply $V_{CC}$. Turns of AUX winding $N_A$ can be calculated as follows:

- $8.5V < \frac{V_{OUT\_MIN}}{N_S} \times N_A < 12V$

**Secondary Rectifier MOSFET Selection**

Under the conditions of $V_{BUS\_MAX}$ and $V_{OUT\_OVP}$, the reverse voltage of the secondary rectification MOSFET will reach its maximum level. The maximum voltage (ignoring the voltage spike) is calculated as follows:

$$V_{D\_R\_MAX} = \frac{\sqrt{2}V_{IN\_MAX}}{N_{PS}} + V_{O\_OVP}$$

Current and $R_{DSON}$ parameters can refer to the following examples:

- For a 20V, 3.3A solution, the BSC098N10NS5 is recommended, which is 100V 8.2mΩ_typ.
- For a 20V, 4.5A solution, the BSC0805LS is recommended, which is 100V 6.0mΩ_typ.
- For a 28V, 5.0A solution, two MOSFETs in parallel are recommended for heat dissipation. For example, two BSC160N15NS5 devices (100V, 13.7mΩ_typ) can be used.

Ensure that the selected MOSFETs can handle the power dissipation under full-load conditions.

# Layout Considerations

Follow these PCB layout guidelines for optimal performance and EMI considerations.

Signals are grouped into two categories:

- Switching nodes:

  Primary side: Drain, AUX, Core

  Secondary side: Drain, AUX, Core

- Sensitive signal nodes (easily affected by interference):

  Primary side: $V_{CS}$, Comp, VSEN, etc.

  Secondary side: REG or TZ (for SY5236), Feedback.

To ensure proper operation, sensitive signal nodes should be routed away from switching nodes. If PCB constraints make this difficult, use static nodes such as $V_{BUS}$, GND, VCC, $V_{OUT}$, SGND, etc as shielding between switching and signal paths.

**To optimize EMI performance:**

- Keep switching node areas on the PCB as small as possible. Avoid using switching nodes (e.g., GaN drain) for heat dissipation.
- Minimize the area of the main current loop.

**Key current loops:**

- Current path during $t_{ON}$: Bus capacitor → Transformer → GaN → $R_{CS}$ → GND → Bus capacitor
- Current path during $t_{OFF}$ time: Transformer → SR_MOS → $C_{OUT}$ → GND → Transformer.
- Leakage inductance and snubber circuit current loop
- Gate drive loops for primary and secondary GaN or MOSFETs

**Component placement guidelines:**

- Place the following components close to the SY50355:
  - COMP capacitor
  - CS resistor (in series)
  - VCC capacitor
- Place the VSEN pull-up resistor near the transformer's AUX pin, and the pull-down resistor near the VSEN pin.
- Place the following components near the SR controller:
  - REG or TZ resistors
  - $V_{DD}$ and $V_{IN}$ capacitors
  -

**GND routing:**

- Connect the GND pin of the SY50355 directly to RCS_GND to ensure an accurate $V_{CS}$ signal and minimize the drive loop area.

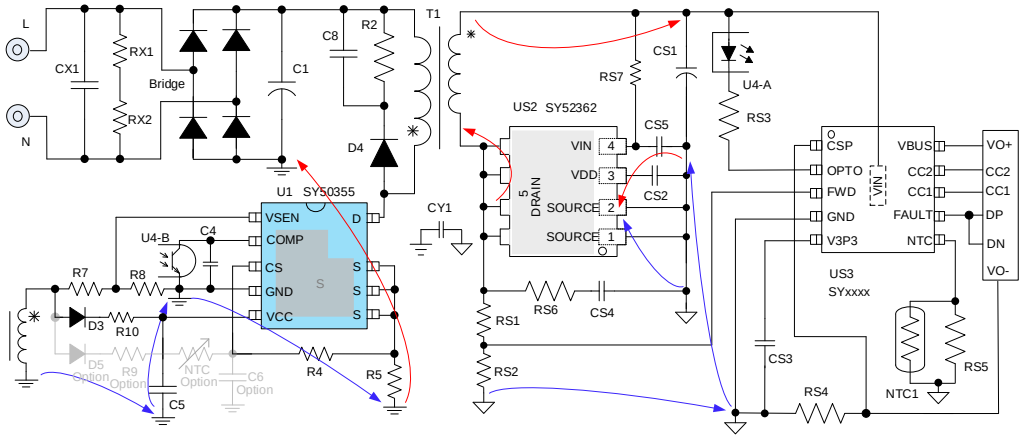



*Figure 9. Recommended PCB Layout*

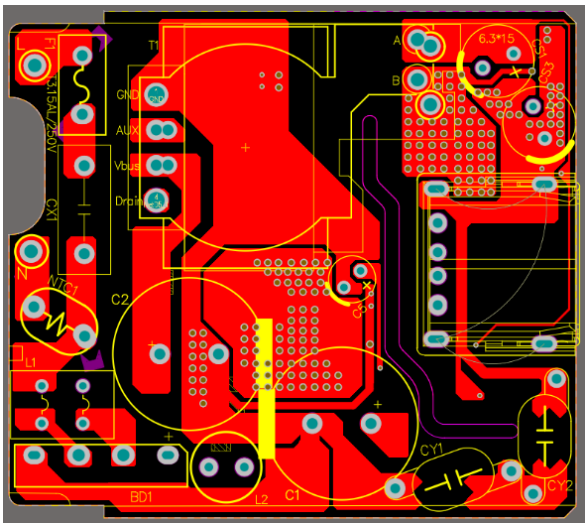


*Figure 10. Top Layer of Recommended PCB Layout (48.0mm * 43.0mm)*

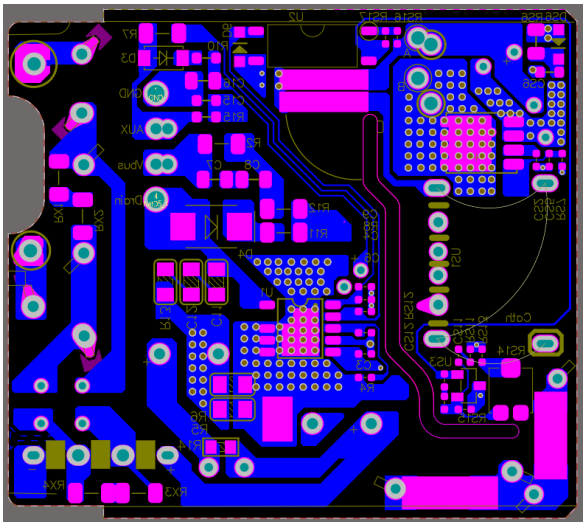


*Figure 11. Bottom Layer of Recommended PCB Layout (Mirrored)*

# Design Example

A step-by-step design example of a typical application is shown below.

### Input/output specifications:

| Parameter | Symbol | Value |
|---|---|---|
| Input voltage range | $V_{IN}$ | AC90V–264V |
| Rated output voltage | $V_O$ | 5V–20V |
| Output OVP level | $V_{O\_OVP}$ | 24V |
| Rated output current | $I_O$ | 3.3A |
| OLP | $I_{OUT\_OLP}$ | 4.0A |
| Efficiency | η | 93% |

### Preset parameters:

| Parameter | Symbol | Value |
|---|---|---|
| The breakdown voltage of power MOS | $V_{MOS\_BR}$ | 700V |
| Secondary diode forward voltage drop | $V_{D\_R}$ | 0V (SR) |
| Transformer effective $A_e$ (ATQ18) | $A_E$ | 62 mm² |

**1. BUS capacitor selection**

Selected BUS capacitor: $C_{BUS}$ = 66μF (1μF/W)

**2. Minimum BUS voltage calculation**

Calculated $V_{BUS\_MIN}$ = 60V

**3. Transformer design**

**(1) Primary-to-secondary turns ratio:** $V_{OR}$=140V, $V_O$=20V, $N_{PS}$=7. $V_{OR} = N_{PS} \times (V_O + V_{D\_F})$

**(2) Select transformer (Ae and Bobbin):** ATQ18, Ae=62mm^2, Winding width=6.0mm.

**(3) Select $N_S$ wire diameter and turns:** 20V 3.3A, ATQ18, Width=6.0mm, 0.10*80mm*1, Ns=4ts.

**(4) Calculate transformer $N_P$:** $N_P$=7*4ts=28ts.

**(5) Calculate Primary Inductance:** $L_P$=195uH (CCM=85kHz, $T_{SW}$=11.8us)

$$L_P = \frac{N_{PS} * V_{BUS_{MIN}}}{I_{OUT_{OLP}} * (V_{OR} + V_{BUS_{MIN}})} * \left(B_{MAX} * A_e * N_P - \frac{V_{OR} * V_{BUS_{MIN}} * T_{SW}}{2 * (V_{OR} + V_{BUS_{MIN}})}\right)$$

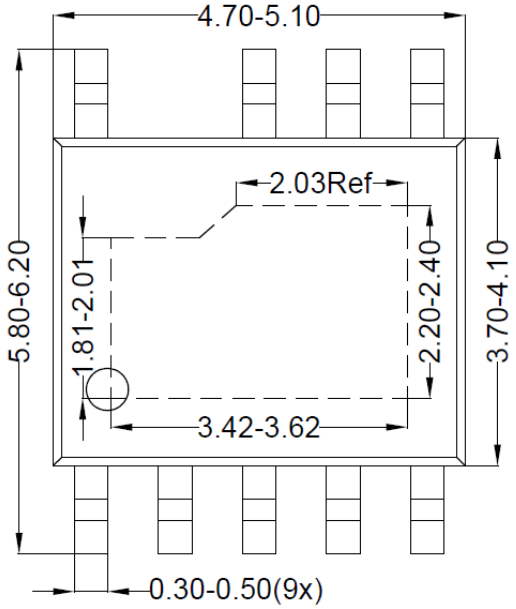
$$L_P = \frac{7 * 60V}{4.0A * (140V + 60V)} * \left(0.37 * 62 * 27ts - \frac{140V * 60V * 11.8us}{2 * (140V + 60V)}\right) = 195uH$$

**(6) Calculate current sense resistor: $R_{CS}$**

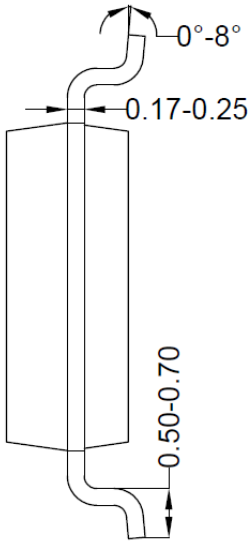
$$R_{CS} = \frac{L_P * V_{CS\_LIMIT}}{B_{MAX} * A_E * N_P} = \frac{195uH * 0.395V}{0.37T * 62mm^2 * 28ts} = 0.12\Omega$$

**(7) Calculate auxiliary winding turns:** $V_{OUT\_MIN}$ = 5V, $N_A$ = 7ts. $8.5V < \frac{V_{OUT\_MIN}}{N_S} \times N_A < 12V.$

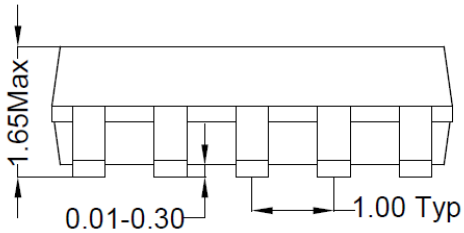
## SSOP9E Package Outline Drawing



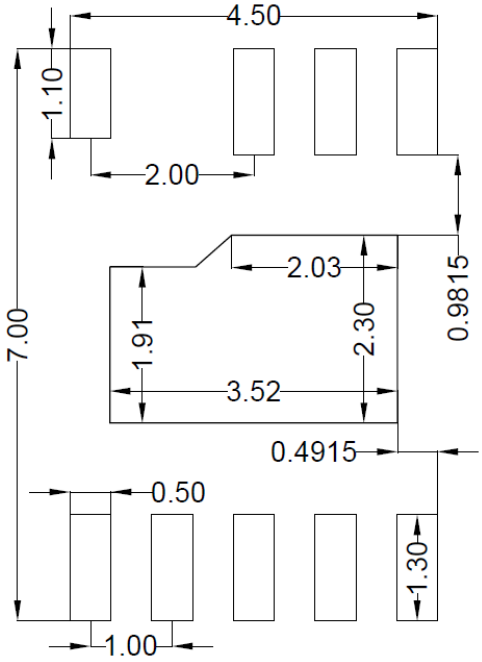

**Top view**




**Side view**




**Front view**

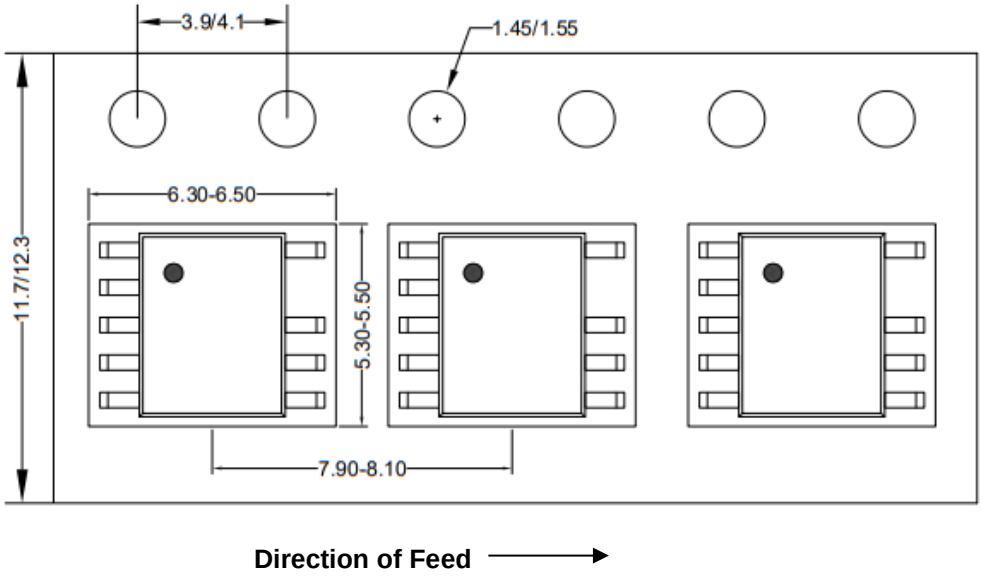



**Recommended PCB layout (Reference only)**

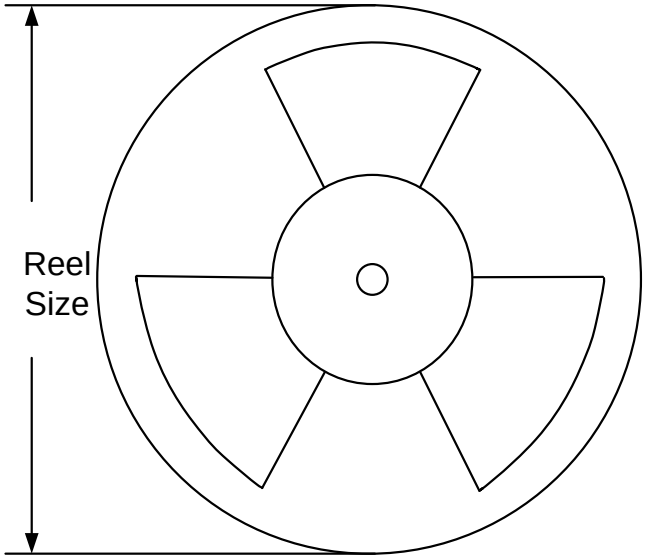
**Notes: All dimension in millimeter and exclude mold flash & metal burr.**

# Tape and Reel Specification

## Tape Dimensions and Pin 1 Orientation




## Reel Dimensions




| Package types | Tape width (mm) | Pocket pitch (mm) | Reel size (Inch) | Trailer * length (mm) | Leader * length (mm) | Qty per reel (pcs) |
|---|---|---|---|---|---|---|
| SSOP9E | 12 | 8 | 13" | 400 | 400 | 4000 |

# Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

| Date | Revision | Change |
|---|---|---|
| December 30,2025 | Revision 1.0 | Initial Release |

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