SY50296/8A

High Frequency QR Flyback Converter with Valley Lockout, Accuracy Output OCP and GaN FET

General Description

The SY50296/8A is a high frequency quasi-resonant (QR) flyback converter designed for Power Delivery (PD) adaptors and quick chargers. It integrated GaN FET in a small package and suitable for wide output voltage range applications. Switching frequency can be 25kHz–500kHz and transformer size can be smaller.

The SY50296/8A operates using peak current control. It provides a QR mode in which the GAN FET can be turned on at a valley point to reduce switching loss, especially under high input voltages.

In conventional QR flyback solutions, the valley number always varies between 1 and 2 or 3 and 5, which increases V_O ripple and creates audible noise. The SY50296/8A uses a proprietary circuit to lock the valley number between 1 and 6, for improved stability compared with other conventional QR solutions.

If load decreases, SY50296/8A will enter discontinuous conduction mode (DCM) to reduce the switching frequency for higher efficiency. If the load is very light, the SY50296/8A will enter burst mode to reduce power loss.

The SY50296/8A provides comprehensive functions to ensure reliable operation, including: HV startup, X-cap discharge, brown-out protection, output and VCC overvoltage protection (OVP), output undervoltage protection (UVP), internal over temperature protection (OTP), and open-loop protection (OLP).

It is recommended to use SY5239 as secondary side Synchronous Rectifier (SR) controller and Zero Voltage Switching (ZVS) can be achieved for higher efficiency.

The SY50296/8A is available in a QFN5*7-18 package.

Features

- Integrated 700V GaN FET
- Programmable Gate Driver Current
- DCM+QR Combined Operating Mode
- Switching Frequency Range: 25kHz–500kHz
- VCCH up to 140V Power Supply
- Automatic Valley Lockout from 1 to 6 Cycles
- Accuracy Output OCP Protection.
- Adaptive OCP (LPS, Limited Power Source)
- Low Frequency Burst (1kHz)
- Frequency Modulation to Reduce EMI Noise
- Internal Soft-Start
- Integrated 700V HV Startup
- X-cap Discharge Protection
- Brown-In/Out Protections
- Programmable Output OVP and UVP
- Current Sense Resistor Short Protection
- Internal and External OTP
- New Package for Excellent Heat Sink.
- MSL3
- Compact Package: QFN5*7-18

Applications

- AC/DC Adapters
- PD Adapters
- Quick Chargers

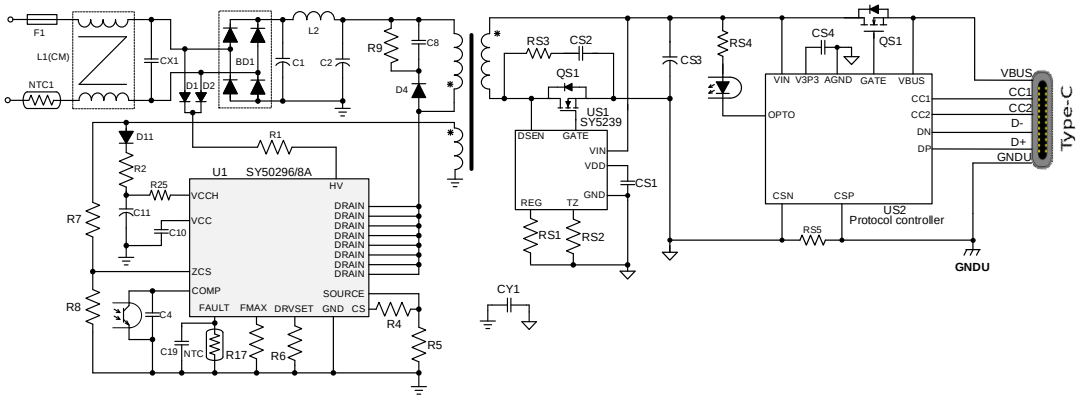


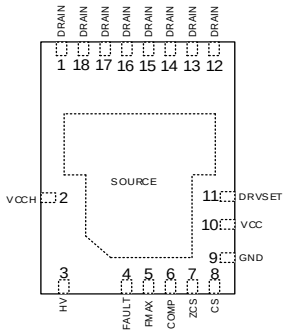
Figure 1. Typical Application Circuit using Synchronous Rectification (SR)

Ordering Information

Ordering Part Number	R_{DSON} (typ)	Output Power	Package type	Top Mark
SY50296AXDQ	0.16Ω	140W	QFN5*7-18	**AAMHxyz**
SY50298AXDQ	0.10Ω	200W	QFN5*7-18	**AAMLxyz**

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1, 12-18	Drain	Drain of internal GaN FET
Bottom Pad	Source	Source of internal GaN FET (Exposed PAD)
4	FAULT	External OTP and Vout OVP pin.
5	FMAX	Maximum switching frequency set.
6	COMP	Compensation voltage of secondary side, connected to an opto-coupler.
7	ZCS	Output voltage, input voltage and QR valley detection pin.
8	CS	Inductor current sensing pin.
9	GND	Ground pin.
10	VCC	Power supply pin.
11	DRVSET	Programmable GaN FET gate drive pin.
2	VCCH	High voltage power supply pin.
3	HV	HV startup, Brown in/out, X-cap discharge pin.

Block Diagram

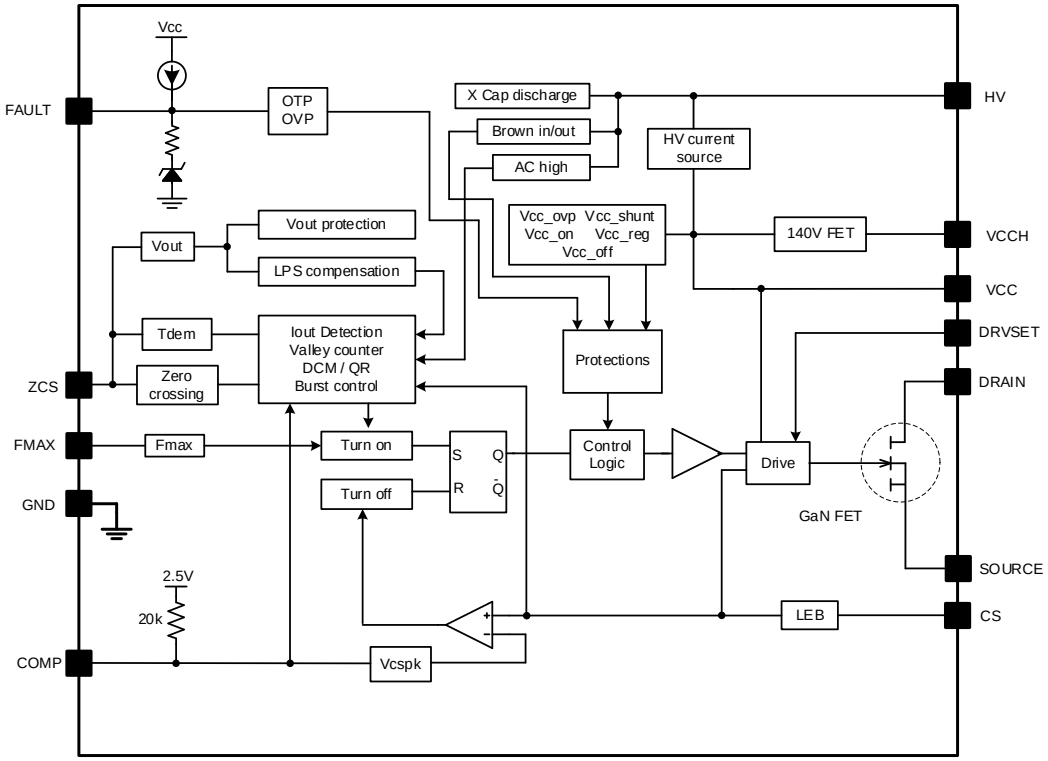


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
Drain	-0.3	700	V
Drain Pulsed Voltage (Intended for repetitive pulse, T_{PULSE} < 100 ns)	-0.3	750	
HV	-0.3	700	
VCCH	-0.3	140	
VCC	-0.3	30	
DRVSET	-0.3	8	
CS, COMP, Fmax, Fault	-0.3	4	
ZCS	-1 (Note 2)	7	
Note2, Dynamic ZCS Negative Voltage in 50μs Duration		-1	V
Note2, Dynamic ZCS Negative Current in 50μs Duration		-2	mA
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature Range	-60	150	
Human Body Model ESD (Drain, HV and VCCH Pin) per ESDA/JEDEC JS-001-2017 (Note 3)		±1	kV
Human Body Model ESD (All Pins Except Drain, HV and VCCH Pin) per ESDA/JEDEC JS-001-2017 (Note 3)		±2	kV
Charged Device Model ESD per JS-002-2018 (Note3)		±500	V
Latch-Up Test per JEDEC78E (Note 3)		±100	mA
MSL Rating		3	

Thermal Information

Parameter (Note 4)	Min	Max	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance		26	°C/W
θ_{JC} Junction-to-Case Thermal Resistance		9	
PD Power Dissipation TA = 25°C		4.8	W

Recommended Operating Conditions

Parameter	Min	Max	Unit
Drain and HV Pin	-0.3	700	V
VCCH	9	140	
VCC	8	25	
CS	-0.3	0.5	
ZCS	-0.3	3.0	
COMP	-0.3	2.5	
Fault	-0.3	3.0	
Junction Temperature Range	-40	125	°C
Case Temperature Range	-40	105	

Electrical Characteristics

(V_{VCC} = 13V (Note 5), T_J = 25°C unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Drain	Break down Voltage	V_{DS_BR}	V_{GS}=0V, I_D=20uA	700			V
	ON Resistance (SY50296A)	R_{DSON}	V_{GS}=6V, I_D=3A ,		0.16	0.21	Ω
	ON Resistance (SY50298A)	R_{DSON}	V_{GS}=6V, I_D=3A		0.10	0.13	Ω
HV	HV Current to Charge VCC	$I_{HV\_CHARGE1}$	V_{HV}=100V_{DC} / Vcc=0V	0.15	0.3	0.55	mA
			V_{HV}=100V_{DC} / Vcc=3V	2.6	4.0	5.4	mA
	AC Unplug Detection Time	t_{UNPLUG_DBC}	Enable X cap function		180		ms
	Current to Discharge X Cap	I_{HV_XCAP}	Enable X cap function		2.0		mA
	AC low or high Detection	$HV_{TH\_AC\_HIGH}$		200	218	236	V
	AC Low Debounce Time	$t_{AC\_LOW\_DBC}$			20		ms
	BO Threshold	HV_{TH_BO}		76	83	90	V
	BO Debounce Time	t_{BO_DBC}			180		ms
	BI Threshold	HV_{TH_BI}			105		V
	BI Debounce Time	t_{BI_DBC}			200		μs
VCCH	Maximum Voltage	$VCCH_{BV}$		140			V
FAULT	Current Source for OTP	I_{OTP}		46.5	49	51.5	μA
	OTP Threshold	V_{OTP_TH}		0.37	0.4	0.43	V
	OTP Exit Threshold	$V_{OTPEXIT\_TH}$			0.45		V
	Clamp Diode for OVP	$V_{OVPDIODE}$		1.1	1.3	1.5	V
	Capability of Clamp Diode	$I_{RFAULTOVP}$			1		mA
	OVP Threshold	V_{OVP_TH}			2.5		V
	Debounce Time of OTP/OVP	$t_{FAULTOTP/OVP\_DBC}$	V_{FAULT}<V_{OTP_TH} V_{FAULT}>V_{OVP_TH}		100		μs
FMAX	Frequency Set	F_{MAX}	R>260kΩ		100		kHz
			R=100kΩ		260		kHz
			R<52kΩ or floating	470	500	530	kHz
VCC	VCC Turn-On Threshold	V_{CC_ON}	V_{CC} rising	18	20	22	V
	VCC Turn-Off Threshold	V_{CC_OFF}	V_{CC} falling	6.5	7.0	7.5	V
	VCC Short Threshold	$V_{CC\_SHORT\_TH}$		0.5	0.7	0.8	V
	Vcc_reg Threshold	V_{CC_REG}		10	11	12	V
	Vcc_reg Hysteresis	V_{CC_REGHYS}			1.0		V
	Protection Timer after Error	t_{ERROR}			1.0		s
	VCC OVP Threshold	V_{CC_OVP}	V_{VCC} rising	26.4	28.0	29.6	V
	VCC OVP Detection	N_{VCCOVP_DBC}			4		pwm
	VCC Shunt Threshold	V_{CC_SHUNT}		25	27	29	V
	VCC Shunt Current	I_{VCC_SHUNT}	V_{CC}>V_{CC_SHUNT}		10		mA
	Normal Operation Current Consumption	$I_{CC\_OPERATING}$	C_L = open, f_{SW} = 50kHz		1.2		mA
	Standby Current	$I_{CC\_STANDBY}$	V_{COMP}<$V_{TH\_SLEEP\_IN}$	280	400	520	μA
CS	Maximum Peak Current Threshold	V_{CS_MAX}	Secondary Side Diode or SR Short	685	720	755	mV
	Leading Edge for V_{CS_MAX}	t_{CS_LEB1}			150		ns
	V_{CS_MAX} Cycles	N_{VCSMAX_DBC}			4		

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
	V_{CS} Limit at AC low input	$V_{CS\_LIMIT\_ACLOW}$		475	500	525	mV
	V_{CS} Limit at AC high input	$V_{CS\_LIMIT\_ACHIGH}$		425	450	475	mV
	Blanking of V_{PK} &V_{CS_LIMIT}	t_{CS_LEB2}			250		ns
	OCP Threshold Normal	$V_{REF\_OCPNORMAL}$		625	660	695	mV
	OCP Threshold LPS	$V_{REF\_OCPLPSL}$	$V_{ZCS}>V_{ZCSLPS\_HIGH}$	515	540	565	mV
	OCP Threshold LPS	$V_{REF\_OCPLPSH}$	$V_{ZCS}<V_{ZCSLPS\_LOW}$	880	925	970	mV
	OCP Debounce Time	$t_{IOUTOCP\_DBC}$			200		ms
	V_{CS} Minimum in DCM	V_{CSMIN_DCM}		110	125	140	mV
	Soft-Start Time	t_{SST}			10		ms
	Frequency Modulation (QR)	$f_{MODULATION\_QR}$			4		kHz
	V_{CSPK} Modulation Amplitude in QR Mode	$V_{QR\_MODULATION1}$	Valley = 1–3		20		mV
			Valley = 4–6		30		mV
	CS Short in Soft Start	V_{CS_SHORT}	t_{ON} = 6.2μs		60		mV
	Current Mirror In Ton	V_{CS_MIRROR}	Izcs:Ics		12:1		/
ZCS	OVP Threshold	V_{ZCS_OVP}		2.36	2.50	2.64	V
	OVP Detection	N_{ZCSOVP_DBC}			4		pwm
	UVP Threshold	V_{ZCS_UVP}			375		mV
	UVP Detection	$t_{VOUTUVP\_DBC}$			20		ms
	Maximum Value of Toff_leb	t_{ZCSLEB_MAX}		1.6	2.3	3.0	μs
	Minimum Value of Toff_leb	t_{ZCSLEB_MIN}		0.65	0.9	1.3	μs
	Maximum Off-Time	t_{OFF_MAX}		210	290	370	μs
	Zero-Cross Point	V_{ZCS_ZERO}			0		mV
	QR Turn-On Delay	$t_{ZCS\_ONDELAY}$			100		ns
	ZCS High Point in LPS	V_{ZCSLPS_HIGH}		1.74	1.90	1.98	V
	ZCS Low Point in LPS	V_{ZCSLPS_LOW}		1.06	1.12	1.24	V
COMP	Internal Pullup Voltage	V_{COMP_PULLUP}		2.2	2.5	2.8	V
	Internal Pullup Resistor	R_{COMP_PULLUP}			20		kΩ
	V_{CS_LIMIT} Point	V_{COMP_LIMIT}			1.9		V
	QR Mode to DCM Change Threshold	V_{COMPTH_DCM}			1.0		V
	Hysteresis of QR Mode to DCM	V_{COMPTH_DCMHYS}			0.1		V
	Minimum Switching Frequency Threshold	V_{COMP_FMIN}		0.55	0.7	0.85	V
	Enter Burst Mode Threshold	$V_{COMP\_BURSTIN}$	V_{COMP} falling	0.19	0.25	0.31	V
	Exit Burst Mode Threshold	$V_{COMP\_BURSTOUT}$	V_{COMP} increasing		0.45		V
	Start PWM Threshold in Burst Mode	$V_{COMP\_BURSTSTART}$	V_{COMP} increasing		0.35		V
	Burst Period	t_{BURST}			1		ms
	OLP Threshold	V_{COMP_OLP}	V_{COMP} rising	1.95	2.2	2.45	V
	OLP Debounce Time	t_{OLP_DBC}	V_{COMP}> V_{COMP_OLP}		90		ms
DRVSET	High Voltage Clamp	V_{DRV-CS_CLAMP}		6.0	6.3	6.6	V
	Programmable Driver Current	I_{DRV}	DVR-GND: 43kohm		5		mA
			DVR-GND: 22kohm		10		mA
			DVR-GND: 10kohm	14	20	26	mA

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
			DVR-GND: <2kohm		Error		
	Sink Current	I_{DRV_SINK}			500		mA
	Maximum Ton	t_{ON_MAX}		18	26	34	μs
	Frequency Limit in DCM	f_{LIMIT_DCM}			75		kHz
	Frequency Minimum in DCM	f_{MIN_DCM}		20	25	32	kHz
	DCM Mode Modulation Frequency	$f_{MODULATION\_DCM}$			250		Hz
	Valley Number in QR Mode	$VALLEY_{NUMBER}$	HV < 218V	1		6	
			HV > 218V	2		6	
Internal OTP	OTP Threshold	$T_{OVP\_SHUNTDOWN}$			150		°C
	Recovery Threshold	$T_{OVP\_RECOVERY}$			130		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Dynamic ZCS Negative Voltage in 50μs Duration.

Note 3: Meets ESDA/JEDEC JS-001-2017 and JEDEC78E.

Note 4: θ_{JA} is measured in the natural convection at TA = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on “2 x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal via to bottom layer ground plane.

Note 5: Increase VCC pin voltage gradually higher than V_{CC_ON} voltage, then reduce it to 13V.

Detailed Description

HV Startup and Power Supply

The HV pin charges the VCC capacitor at AC power-on. When VCC voltage rises above the startup threshold, the HV circuits will be turned off to reduce power loss.

HV will charge the VCC and VCCH pins together during AC power-on. The suggested value for the VCCH and VCC capacitors are 10μF and 1μF, respectively which enables a small total solution size.

In situations when the device enters protection mode, the PWM operation is stopped for a t_{ERROR} time. Because of the power consumption during t_{ERROR}, the VCC and VCCH capacitor voltages will drop. When VCC falls to V_{CC_REG}, HV circuitry is enabled again to charge the capacitors until VCC > (V_{CC_REG} + V_{CC_REGHYS}). After t_{ERROR}, the internal logic will be reset, and a restart sequence is initiated.

QR Mode (Automatically Selected Valley Number between 1 and 6)

In QR mode, PWM turns on at the valley point of the GAN FET drain voltage. This improves EMI and efficiency. V_{CSPK} is controlled by V_{COMP}, and the valley number is controlled by the output load. When V_{COMP} is higher than (V_{COMP_THDCM} + V_{COMPTH_DCMHYS}), QR mode is enabled and on the 6th valley number. As the load increases, the valley number decreases in one-step increments until it reaches the minimum value.

Valley Detect

The waveform in Figure 3 shows the valley detection method. When the falling edge of the zero-crossing voltage appears at the ZCS pin, the SY50296/8A will turn on the GAN FET after a delay.

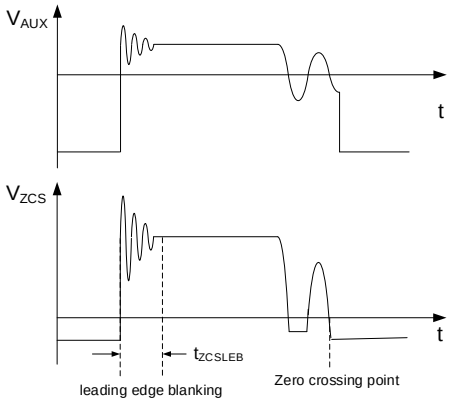


Figure 3. Valley Detection

Noise is present at the ZCS pin when the GAN FET turns off, which may affect valley detection. The SY50296/8A uses a blanking time to avoid noise interference, which is described in the Output OVP and UVP section.

DCM Mode

When V_{COMP} is lower than V_{COMPTH_DCM}, DCM mode is enabled. In DCM mode, V_{CSPK} and the switching frequency is controlled by V_{COMP}. PWM turns on instantly at f_{SW} and does not wait for the valley point. As load decreases, frequency first decreases from f_{LIMIT_DCM} to f_{MIN_DCM}, and the part operates in PFM mode to maintain high efficiency. When the frequency has decreased to F_{MIN_DCM} and load continues decreasing, V_{CSPK} begins decreasing to keep constant output voltage.

Burst Mode

When frequency and V_{CSPK} have all decreased to respective minimum values, if the output load continues decreasing, V_{COMP} will be lower than $V_{COMP\_BURSTIN}$. In this case the device starts operating in Burst mode. PWM will start when V_{COMP} is higher than $V_{COMP\_BURSTSTART}$. The PWM number of switching cycles is controlled by t_{BURST} in order to keep burst frequency lower than the set value. PWM operation will continue until the set number cycles are completed. PWM then stops and waits for the next rising edge of $V_{COMP\_BURSTSTART}$. With this method, the burst frequency is low and audible noise is reduced.

When V_{COMP} is higher than $V_{COMP\_BURSTOUT}$, the SY50296/8A will enter DCM mode.

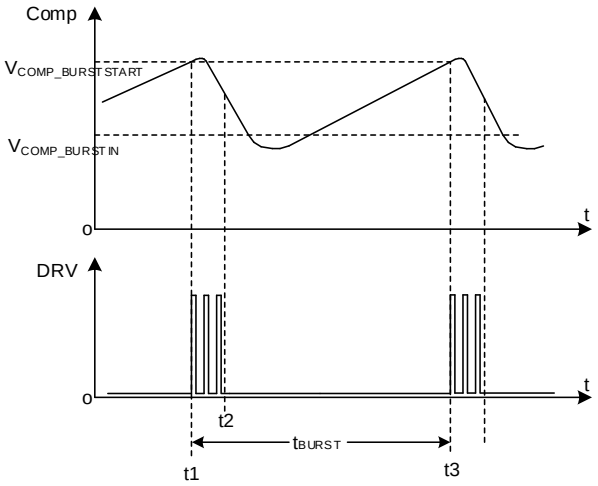


Figure 4. Quiet Burst

VCCH Power Supply

In order to simplify external circuits, the SY50296/8A includes an internal LDO connected to the VCCH pin with a maximum voltage of up to 140V. When VCC is lower than V_{CC_REG}, VCCH will charge the VCC capacitor through an internal circuit. When VCC is higher than (V_{CC_REG} + V_{CC_REGHYS}), VCCH will stop charging.

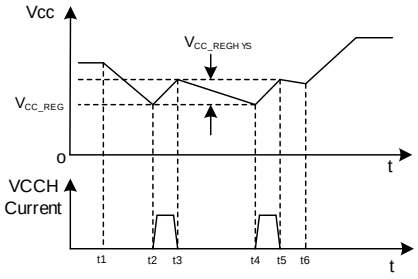


Figure 5 VCCH Charge Function

If high efficiency is important and slightly increasing the BOM cost is acceptable, two windings can be used to reduce VCC loss. As shown in Figure 6, if V_{OUT} is low, Na3 voltage is too low and VCCH charges VCC. If V_{OUT} is high, Na3 voltage is high enough and VCCH will be floating. A resistor and Zener diode in parallel with C11, can be used to clamp the high voltage coming from Na1's leakage inductance. The recommended value for R25 is 1kΩ. D25's clamp voltage should be higher than Na1 voltage and lower than C11 rated voltage.

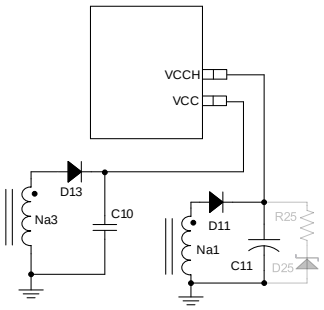


Figure 6. Typical Circuit for High Efficiency Application

Figure 7 shows a single winding solution. The recommended value for C10 is 1μF. The parallel resistor and Zener diode for C11 are not needed.

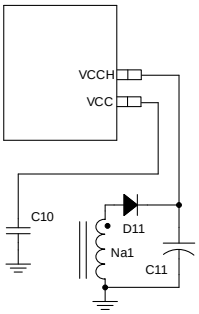


Figure 7. Typical Circuit for One Winding Application

Accuracy Output Over Current Protection (OCP)

The SY50296/8A detects output current at primary side. Before PWM turn off instant, CS pin samples voltage on Rcs. When current of Ns winding falls to zero, ZCS pin records demagnetization time. With these two signals, SY50296/8A calculates output current and the result is compared with Vref_ocp (Internal threshold). When the result is higher than Vref_ocp for $t_{IOUTOCP\_DBC}$, PWM stops and timer begins. After t_{ERROR}, logic will be reset and HV will charge Vcc to V_{CC_ON} for restart.

Iout_ocp can be set by Rcs with following formula. Vref_ocp is internal voltage of SY50296/8A. Nps is Np/Ns of transformer. Rcs is R5 in following circuit.

$$I_{OUT\_OCP} = \frac{0.93 * V_{RER\_OCP} * N_{PS}}{6 * R_{CS}}$$

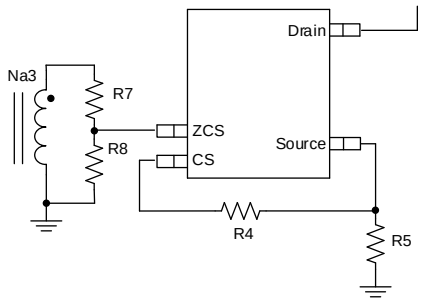


Figure 8. Typical Circuit for Rcs calculation

R4 is used to compensate Iout_ocp. If Iout_ocp becomes higher according to input voltage's increase, R4 should be added. If Iout_ocp falls according to input voltage's increase, R4 should be reduced. R4 range may be 100ohm to 500ohm.

Output OCP Modes

In quick charge applications, Vout range is usually very wide, such as 3.3V to 21V. Iout range is very wide too. SY50296/8A has two OCP options to different applications.

The first example is Normal OCP mode. Output voltage and current include 5V/3A, 9V/3A, 12V/3A, 15V/3A, 20V/3.25A, 3.3V-21V/3A. Normal OCP option is suitable. VREF_OCPNORMAL is changeless according to different output voltages.

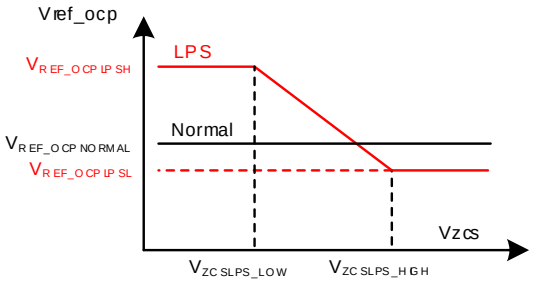


Figure 9. Two Output OCP modes

The second example is LPS OCP mode. Output voltage and current include 5V/3A, 9V/3A, 10V/6.5A, 12V/5A, 15V/4A, 20V/3.25A, 5V-12V/5A. If Normal OCP option is adopted, OCP value should be higher than 6.5A and maybe set to 7.0A. When Vout is changed to 20V, Iout_ocp is still 7.0A and maximum output power will be 140W. This is forbidden in UL60950.

The SY50296/8A's LPS option is suitable for the second example. V_{REF_OCPLPS} is related to Vout. Iout_ocp can be set by Rcs when Vout is highest voltage. When Vout is lower, V_{REF_OCPLPS} becomes higher. At Vout=10V, Iout_ocp is higher than 6.5A and 10V 6.5A won't trigger output OCP.

Output OCP and X cap by the ZCS Resistor

Output OCP functions can be selected using the ZCS resistor. ZCS resistors configuration:

ZCS Pulldown	X Capacitor	Output OCP
25-27kOhm ±1%	Disabled.	Normal Option
13.0kOhm ±1%	Enabled.	Normal Option
7.5kOhm ±1%	Disabled.	LPS Option
3.0-3.6kOhm ±1%	Enabled.	LPS Option

The ZCS_OVP threshold is 2.50V. With R8 selected, R7 can be calculated according to V_{OUT_OVP} and Na/Ns.

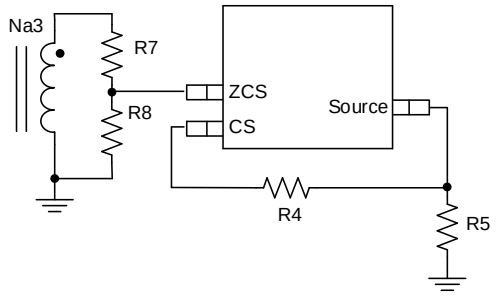


Figure 10. Output OCP and X cap by ZCS Resistor

Programmable Drive Current

At turn on instant, SY50296/8A uses constant current to charge Cgs of M1 and EMI performance is improved. At turn off instant, DRVSET pin will be fast pulled down to reduce turn off loss.

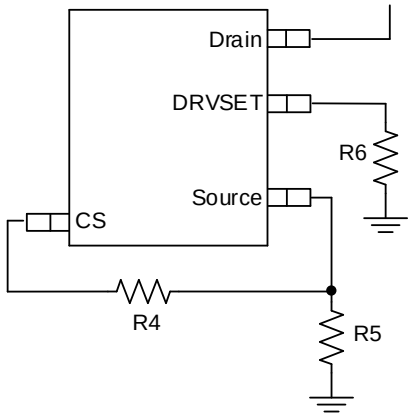


Fig.11 Drive circuit of GaN FET

Constant current value at turn on instant can be selected by R6. When current is lower, GaN's turn on speed will be slower and EMI performance will be better. Table is as follows. At SY50296/8A's startup, R6 is detected and current is fixed until startup again.

R6	Constant current
10kohm	20mA
22kohm	10mA
43kohm	5mA
<2kohm	No PWM

Fig.12 Drive current table

Frequency Limitation

To QR mode operation, when load decreases, switching frequency will increase and switching loss will increase too. Fmax pin can be used to limit maximum frequency. Relationship between frequency limitation and Fmax pin resistor is shown as follows.

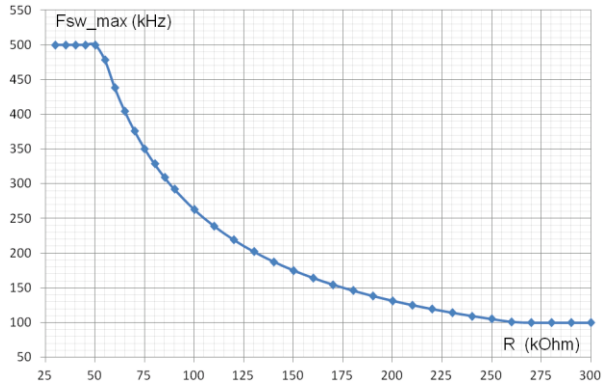


Fig.13 Frequency limitation

When Fmax pin is floating, frequency limitation is 500kHz. If the resistor is lower than 30kOhm, frequency limitation is 500kHz too. When frequency limitation is triggered, PWM will turn on at the valley after limitation.

Frequency Modulation

In QR mode, the SY50296/8A adds a triangle voltage on V_{CS} for frequency modulation. If the valley number is between 1 and 3, the modulation amplitude is set to 20mV. If the valley number is between 4 and 6, the modulation amplitude is set to 30mV in order to obtain an effective range of frequency modulation.

Soft-Start

At startup, when V_{COMP} rises to $V_{COMP\_BURSTSTART}$, PWM operation starts and V_{CS} increases from the minimum value linearly. Under heavy load or V_{OUT} short conditions, soft-start will terminate after t_{SST}. Under light load or no-load conditions, when the V_{CS} value determined by V_{COMP} is lower than the value determined by soft-start, soft-start will terminate and V_{COMP} will control V_{CS}.

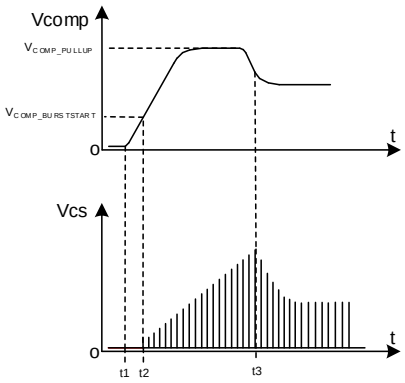


Figure 14. Soft-Start Process

Under startup or V_{OUT} short conditions, V_{OUT} and ZCS are very low. If ZCS cannot detect an effective valley signal, t_{OFF_MAX} will be enabled. This is helpful to reduce deep CCM switching and reduce the voltage stress on the SR MOSFET V_{DS}.

V_{CS_LIMIT}

After t_{CS_LEB2} in every cycle, when V_{CS} is higher than V_{CS_LIMIT}, PWM will turn off immediately. The decision is made cycle by cycle and won't affect next cycle's PWM on time.

V_{CS_MAX} Protection

Under normal operating conditions, V_{CS_LIMIT} can limit GAN peak current and provide sufficient protection. When the transformer winding or the secondary diode short circuits, the current slope is very high and the transformer will enter saturation state. The current can rise to a much higher level during t_{CS_LEB2}.

The SY50296/8A can detect V_{CS} after t_{CS_LEB1}, which is shorter than t_{CS_LEB2}. If V_{CS} is higher than V_{CS_MAX} for four consecutive cycles, PWM operation stops and the timer starts. After t_{ERROR}, the logic is reset and a restart is triggered, with HV charging VCC to V_{CC_ON}.

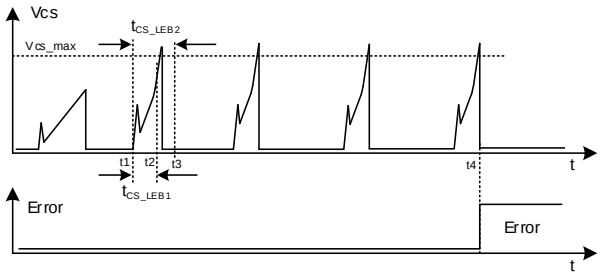


Figure 15. V_{CS_MAX} Process

Brown-In and Brown-Out

When input voltage is lower than 90V AC, current and heat dissipation on the transformer and primary GAN FET are very high. The SY50296/8A provides brown-in (BI) and brown-out (BO) protections to protect the power supply. Brown-in and brown-out are defined as follows:

- BI: HV voltage is higher than $HV_{TH,BI}$ and lasts for t_{BI_DBC}.
- BO: HV voltage is lower than $HV_{TH,BO}$ and lasts for t_{BO_DBC}.

After a BO event, PWM stops. After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON}.

X-cap Discharge

Under light load, when charger is unplugged from AC socket, there may be remaining high voltage on input terminal, which is dangerous to be touched.

The SY50296/8A uses HV to discharge X-cap. HV pin is connected to AC side through R1, D1 and D3. R1 is recommended to be 5k – 10kOhm, which can provide more reliability against surge voltage on AC line.

If HV hasn't rising edge for continuous T_{UNPLUG_DBC}, AC unplug is detected. PWM stops and timer begins. HV sinks current of I_{HV_XCAP} to Vcc pin. Vcc rises to V_{CC_SHUNT} and HV falls linearly. When HV can't supply Vcc and Vcc is lower than V_{CC_OFF}, discharge will stop.

Voltage rating of Vcc capacitor should be higher than Vcc_shunt. Then 35V capacitor is recommended.

During X-cap discharge, once HV detects rising edge, which means AC re-plug happens, the discharge will be terminated immediately. Timer of t_{ERROR} will go on. During t_{ERROR}, HV will keep Vcc between V_{CC_REG} and (V_{CC_REG}+V_{CC_REGHYS}). After t_{ERROR}, logic will be reset and HV will charge Vcc to V_{CC_ON} for restart.

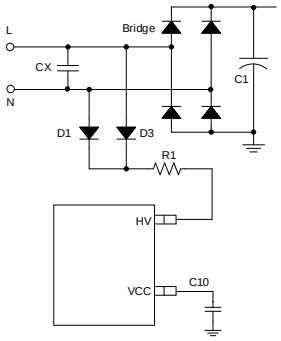


Fig.16 X-cap discharge circuit

Following waves show the process.

At t1, AC unplug happens.

At t2, AC unplug is confirmed. PWM stops and HV sinks current to Vcc.

At t3, Vcc rises to V_{CC_SHUNT}.

At t4, X-cap discharge current is lower than Vcc's dissipation and Vcc begins falling.

At t5, Vcc is lower than V_{CC_OFF} and discharge is reset.

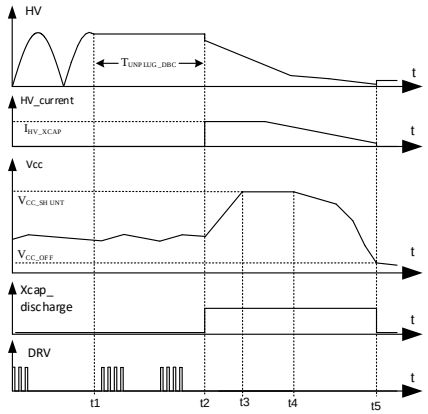


Fig.17 X-cap discharge waveforms

Output OVP and UVP

The SY50296/8A detects the output voltage through the ZCS pin and provides output overvoltage protection (OVP) and undervoltage protection (UVP). When the primary GAN FET turns off, there is a parasitic resonance on AUX winding. The SY50296/8A uses blanking time to avoid false triggering. Blanking time is adaptive according to V_{CSPK}. When V_{CSPK} is below 200mV, primary current is low and energy stored in leakage inductance is also low. Parasitic resonance on auxiliary winding will be shorter, and blanking time is also shorter. Blanking time increases to the maximum value as V_{CSPK} rises to 500mV.

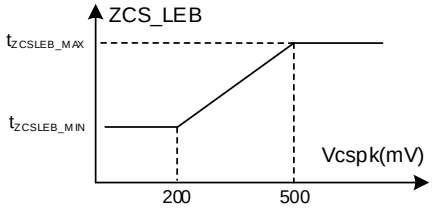


Figure 18. ZCS Blanking Time

When ZCS voltage is higher than V_{ZCS_OVP} for N_{ZCSOVP_DBC} cycles, ZCS_OVP is triggered and PWM stops. After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON}.

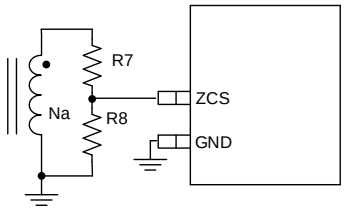


Figure 19. ZCS OVP Setting

Output OVP threshold is calculated as follows:

$$V_{OUT\_OVP} = V_{ZCS\_OVP} \times \frac{R7 + R8}{R8} \times \frac{Ns}{Na}$$

When ZCS voltage is lower than V_{ZCS_UVP} continuously for a $t_{VOUTUVP\_DBC}$ period, ZCS_UVP is triggered and PWM stops. After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON}.

Note: The pulldown resistor R8 value should be selected first, based on Output OCP settings. Then, R7 should be calculated according to the above equation. UVP is used to avoid continuous operation under V_{OUT} short circuit conditions and is not mandatory for the design.

VCC OVP

The SY50296/8A provides VCC overvoltage protection (OVP) to protect the IC from abnormal high voltage caused by an open feedback loop or improper N_A winding. When VCC rises to V_{CC_SHUNT} and external power current capability is higher than the shunt ability, VCC can continue rising.

VCC is continuously monitored. If VCC is higher than V_{CC_OVP} for four continuous cycles, VCC OVP is triggered and PWM stops. After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON}.

If the error condition still exists after restart, the IC will operate in hiccup mode.

Open-Loop Protection

If the output is short-circuited, the optocoupler circuit is open, or the load increases too much, V_{COMP} will increase. When V_{COMP} is higher than V_{COMP_OLP} and lasts for t_{OLP_DBC}, open-loop protection (OLP) is triggered and PWM stops. After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON}.

Fault OTP & OVP

Fault pin can be used as OVP and OTP functions. Outside circuit is as follows. At normal state, current of Iotp is clamped by D12. D12's clamp voltage is between OTP threshold and OVP threshold. So, both protections won't be triggered.

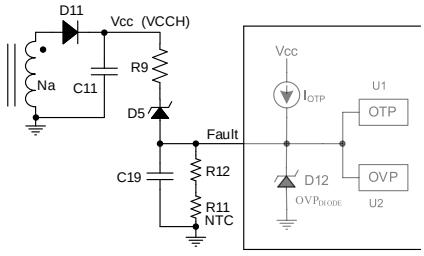


Fig.20 Fault OTP & OVP

Under error conditions, Vcc or VCCH will rise. D5 may be broken down. If pull up current is higher than D12's clamp ability, Fault voltage will be pulled up. When Fault pin is higher than V_{OVP_TH} and last for $T_{FAULTOTP/OVP\_DBC}$, Fault_ovp is triggered. PWM stops and timer begins. After

t_{ERROR}, logic will be reset and HV will charge Vcc to V_{CC_ON} for restart.

R11 is NTC resistor. As temperature's rising, R11's resistance falls. When R11 is small enough, there will be no current flowing into D12 and all the current of Iotp will flow into R11. As Iotp is changeless, Fault voltage will fall along with R11's resistance. When Fault voltage is lower than V_{OTP_TH}, Fault_otp is triggered. PWM stops and timer begins. After t_{ERROR}, logic will be reset and HV will charge Vcc to V_{CC_ON} for restart. After restart, Fault pin is detected. PWM won't begin until Fault is higher than $V_{OTPEXIT\_TH}$.

R9 is used to limit the current flowing into Fault pin. OVP threshold is mainly decided by D5's breakdown voltage. R12 is used to adjust OTP threshold conveniently. C19 is used to filter various noise and recommended value is 100pF.

CS Short Circuit

During t_{ON} of every PWM cycle in soft start process, V_{CS} is sampled every 6.2μs and compared with V_{CS_SHORT}. If $V_{CS} < V_{CS\_SHORT}$, short-circuit protection is triggered and PWM stops. After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON}. This protection is only enabled in soft start.

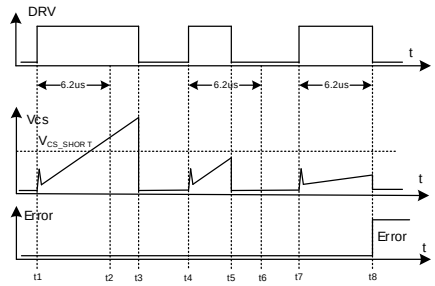


Figure 21. CS Pin Short Protection

- At t2, V_{CS} is higher than V_{CS_SHORT}. No protection.
- At t5, the 6.2μs timer has not expired. No comparison is needed. No protection.
- At t8, V_{CS} is lower than V_{CS_SHORT} at 6.2μs mark. Protection is triggered.

Internal OTP

The SY50296/8A continuously monitors the die temperature during normal operating. When the die temperature rises above the OTP threshold, PWM stops. After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON}.

Design Guide

BUS Capacitor Calculation

Generally, bulk capacitor CBUS is selected according to the following rules:

- No PFC: 1.5–1.8uF per watt (Output power).
- With PFC: 0.5–0.8uF per watt (Output power).

Minimum BUS Voltage Calculation

Minimum BUS voltage appears when input voltage V_{AC} is lowest and output current reaches its rated value. When there is no power factor correction (PFC) circuit before the flyback, minimum BUS voltage is calculated as follows:

$$V_{BUS\_MIN} = \sqrt{2V_{IN\_MIN}^2 - \frac{P_O(1-K_{CH})}{\eta C_{BUS} f_o}}$$

where K_{CH} is the BUS capacitor charge coefficient (generally K_{CH} is set to 0.2–0.3), η is conversion efficiency, and f_o is the AC input frequency.

When selecting the necessary capacitors, the following aspects have to be considered: The actual capacitance for aluminum capacitors is only 85-90% of nominal value and component tolerance has to be taken into account.

The following examples are helpful for fast selection and can be used as a reference.

For a 30W solution, with no boost PFC circuit. Bus nominal capacitance is 27 + 27μF. V_{BUS_MIN} is as follows:

Output Power	30W	35W	40W	45W
AC90V 50Hz	86V	80V	75V	68V
AC90V 60Hz	93V	87V	83V	78V

For optimal performance, V_{BUS_MIN} should be higher than 80V.

For a 66W solution, no boost PFC circuit. Under full load 20V, 3.3A, V_{BUS_MIN} is as follows:

Bus Nominal Capacitance	82+22μF	82+10μF	82μF	68μF
AC90V 50Hz	82V	78V	72V	60V

For optimal performance, V_{BUS_MIN} should be higher than 80V.

For a 140W solution, boost + flyback topology. Output is 28V, 5A. Bus nominal capacitance is 39+39uF.

At AC90V 50Hz, boost PFC outputs DC240V. V_{BUS} is 222V (min) to 253V (max). Ripple is 31V.

At AC176V 50Hz, boost PFC outputs DC350V. V_{BUS} is 338V (min) to 362V (max). Ripple is 24V.

Transformer Parameters Calculation

1. Primary/secondary turns ratio: N_{PS}

N_{PS} is limited by voltage stress on the primary GAN FET

$$N_{PS} \le \frac{V_{GAN\_BR} * K_{DR} - \sqrt{2} * V_{IN_{MAX}} - \Delta V_{SN}}{V_O + V_{D\_F}}$$

where V_{GAN_BR} is the breakdown voltage of the primary GAN FET; K_{DR} is the V_{DS} de-rating factor of the power GaN; $V_{IN,MAX}$ is always AC264V; V_{D_F} is the forward

voltage of the secondary rectification diode (If SR is used on the secondary side, use V_{D_F} = 0); ΔV_{SN} is the voltage spike at primary GaN turn-off. A starting value of 50V can be used for the calculation.

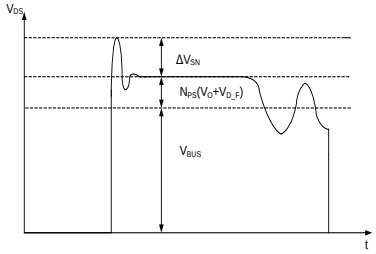


Figure 22. Primary V_{DS} Waveform

After N_{PS} is determined, the reflected voltage can be calculated as follows:

$$V_{OR} = N_{PS} \times (V_O + V_{D\_F})$$

Typical value of V_{OR} is about 120-170V.

2. Primary Rcs

The SY50296/8A has accuracy output OCP function. Rcs is firstly decided by the following formula.

$$R_{CS} = \frac{0.93 \times V_{REF\_OCP} \times N_{PS}}{6 \times I_{OUT\_OCP}}$$

where V_{REF_OCP} is internal threshold, I_{OUT_OCP} is OCP threshold, which is selected based on the maximum output current. For example, if the maximum current required is 3A, then 3.3A can be used for I_{OUT_OCP}

3. Turns of secondary winding: N_S

(a) Select transformer and AE.

(b) Determine winding width of the bobbin.

(c) Select N_S wire gauge

(d) Determine N_S.

N_S may be 3ts to 8ts. To PCB winding, N_S may be 2ts. N_S should be as more as possible for better efficiency.

4. Turns of primary winding: N_P

$$N_P = N_S * N_{PS}$$

5. Calculate maximum primary peak current

$$I_{PPK\_MAX} = \frac{V_{CS\_LIMIT}}{R_{CS}}$$

where V_{CS_LIMIT} is 0.5V.

6. Select B_{MAX} for the magnetic core (0.35T–0.37T)

7. Calculate inductance: L_P(uH)

$$L_P = \frac{N_P \times B_{MAX} \times A_E}{I_{PPK\_MAX}}$$

where A_E is in mm^2 and I_{PPK_MAX} is in A.

8. Turns of auxiliary winding: N_A

For fast charge applications, V_{OUT} range is wide. Turns of AUX winding should take V_{OUT_MAX} and V_{OUT_MIN} into consideration.

In low-cost applications, one winding is enough. The number of turns for the AUX winding can be calculated as follows.

- AUX can supply VCCH at V_{OUT_MIN}.
- $9V < \frac{V_{OUT\_MIN}}{N_S} \times N_{AUX}$
- VCCH should be less than 120V at V_{OUT_MAX}.
- $\frac{V_{OUT\_MAX}}{N_S} \times N_{AUX} < 120V$

N_{AUX} should be as low as possible. Then power dissipation can be lower.

With this procedure, f_{SW_MIN} is not an input parameter. When L_P is calculated, the switching frequency f_{SW} is determined as well. This will always lead to a satisfactory design, and efficiency will always be close to optimal for a given transformer.

Secondary Rectifier MOSFET Selection

Under the conditions of V_{BUS_MAX} and V_{OUT_OVP}, the reverse voltage of the secondary rectification MOSFET will reach its maximum level. The maximum voltage (ignoring the voltage spike when the primary GaN FET is turned on) is calculated as follows:

$$V_{D\_R\_MAX} = \frac{\sqrt{2}V_{IN\_MAX}}{N_{PS}} + V_{O\_OVP}$$

Maximum instantaneous forward current is calculated as follows:

$$I_{SPK\_MAX} = I_{PPK\_MAX} \times N_{PS}$$

For a 66W (20V, 3.3A) solution, BSC098N10NS5 is recommended, which has 100V, 8.2mΩ (V_{GS} = 10V) ratings.

For a 90W (20V, 4.5A) solution, BSC0805LS is recommended, which has 100V, 6.0mΩ (V_{GS} = 10V) ratings.

For a 120W (20V, 6.0A) solution, two MOSFETs in parallel are recommended, primarily for heat dissipation. Using two BSC098N10NS5, which is 100V, 8.2mΩ (V_{GS} = 10V) ratings.

Ensure that the MOSFET selected can handle the dissipated heat without exceeding the target acceptable temperature increase. Validate the design performing temperature measurements under worst case load and ambient temperature conditions.

Layout Considerations

Follow these PCB layout guidelines for optimal performance and EMI considerations:

Signals are grouped in two categories:

- Switching nodes: primary drain/AUX/core; secondary drain/AUX/core.
- Important signal nodes (easy to be disturbed):
  - Primary: CS, Comp, ZCS, Fmax, etc.
  - Secondary: REG, TZ (TZ pin of SY5239), feedback loop, etc.
- To guarantee normal operation, important signal nodes should be far away from switching nodes. If PCB routing is difficult, static nodes should be used as shielding between switching and signal nodes. Static nodes can be V_{BUS}, GND, VCC, VCCH, V_{OUT}, SGND, etc.
- In order to optimize EMI performance, switching nodes on the PCB layout should be as small as possible. Switching nodes should not be selected for heat sinking, such as GaN drain.
- In order to obtain good EMI effect, the main current loop should be as small as possible.
  - Current path during t_{ON}: bus capacitor → transformer → GaN → R_{CS} → GND → bus capacitor
  - Current path during t_{OFF} time: transformer → SR_MOS → C_{OUT} → GND → transformer
  - Current in leakage inductance and snubber circuit
  - Drive loop of secondary MOSFET.
- Place these components near SY50296/8A:
  - Comp capacitor, Rcs, VCC capacitor.
  - ZCS pullup resistor should be placed near the AUX pin of the transformer, and pulldown resistor should be near the ZCS pin.
- The REG and TZ resistors, V_{DD} and V_{IN} capacitors should be close to SY5239.
- GND routing is as follows:
  - SY50296/8A's GND should be connected to R_{CS}_GND in order to get accurate V_{CS} signal.

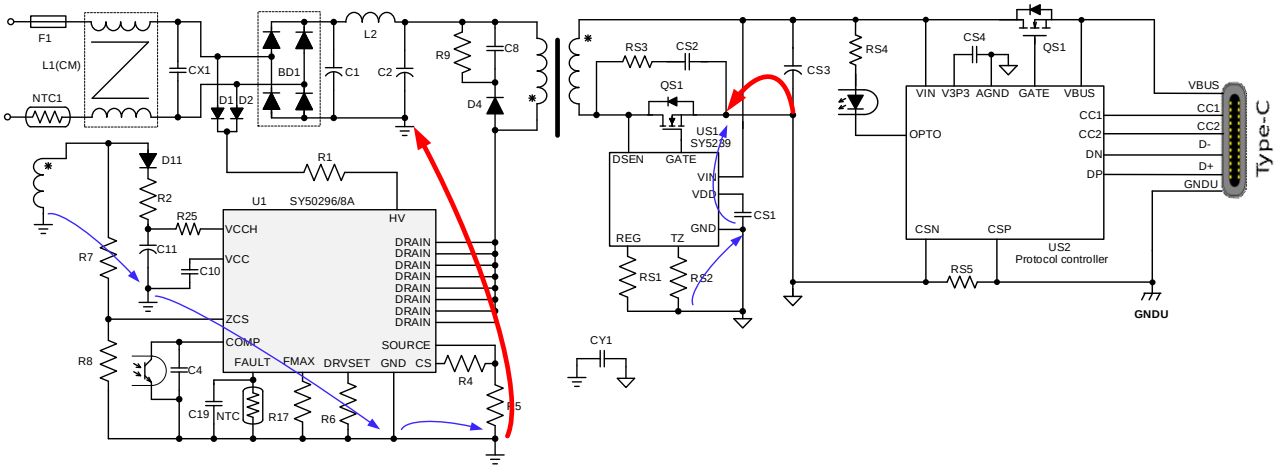


Figure 23. Recommended PCB Layout

As Vgs(th) of GaN FET is as low as 1.2V, it is easy to be falsely triggered by noise.

- **IC_GND should be connected to Rcs_GND directly.**
- **Drive loop should be as small as possible.**

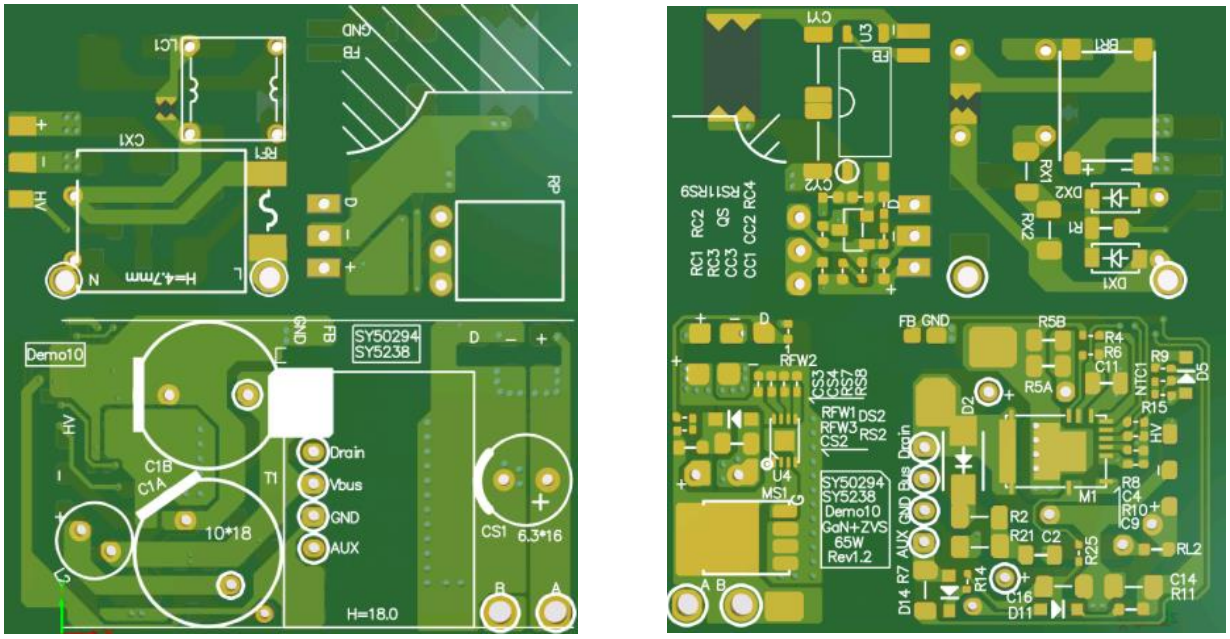


Figure 24. Recommend PCB layout in 3D view.

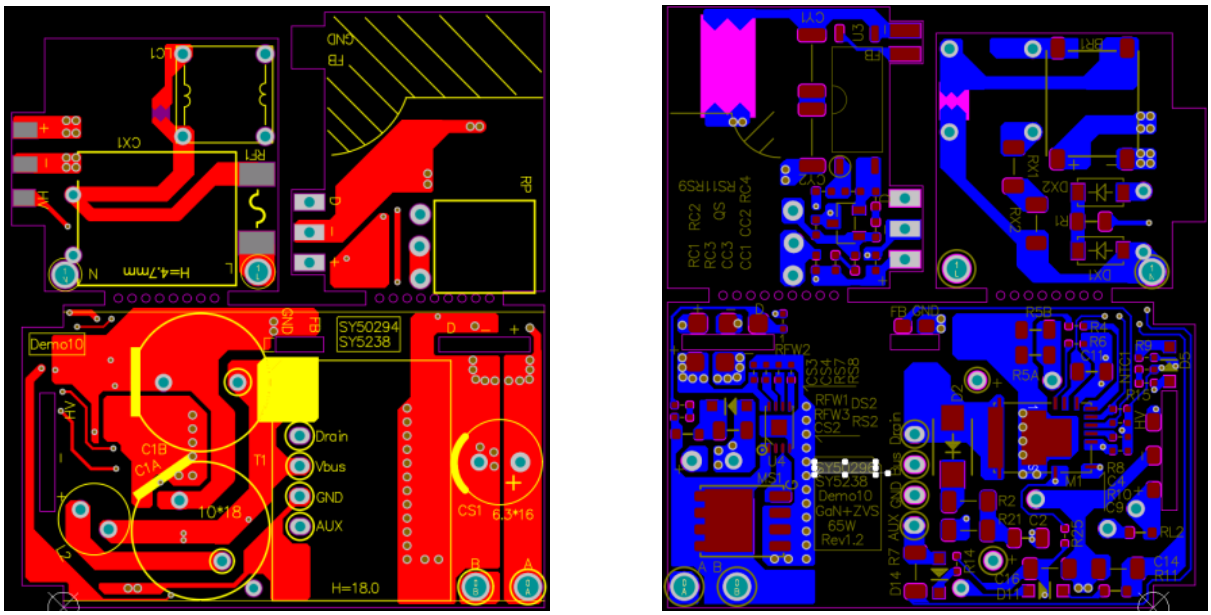


Figure 25. Recommend PCB layout in 2D view.

Design Example

A step-by-step design example of a typical application is shown below based on SY50296A.

Input/output specifications

Parameter	Symbol	Value
Input voltage range	V_{IN}	AC90V – AC264V
Rated output power	P_O	66W
Rated output voltage	V_O	5V–20V
Output OVP level	V_{O_OVP}	24V
Rated output current	I_O	5A
Output OCP	I_{OCP}	5.5A
Efficiency	η	93%

Preset parameters

Parameter	Symbol	Value
Breakdown voltage of power GaN	V_{GaN_BR}	700V
V_{DS} de-rating factor of power GaN	K_{DR}	90%
Spike on V_{DS} at power GaN turn-off	ΔV_{SN}	100V
BUS capacitor charge coefficient	K_{CH}	0.2
Secondary diode forward voltage drop	V_{D_R}	0V (SR)
Transformer effective Ae	A_E	62 mm^2

1. BUS capacitor selection

Select BUS capacitor: C_{BUS} = 104μF (1.57uF/W)

2. Minimum BUS voltage

V_{BUS_MIN} = 84V

3. Transformer design

(1) Transformer core: RM8, Ae=62mm^2

(2) Winding width of bobbin: 9.2mm

(3) Ns Winding wire: 0.10mm*100

(4) Ns=6ts

(5) N_{PS} is selected as: N_{PS} = 6, Reflected voltage V_{OR} = 6 × 20V = 120V.

(6) Np is calculated as: Np=Nps*Ns=36ts

(7) Np wire: 9.2mm*90%/19ts=0.435mm (19ts is by sandwich winding). Wire is 0.40mm or Litz line of 0.10mm*10~15.

(8) Calculate R_{CS}: In normal OCP mode, V_{REF_OCP} = 0.66V.

$$R_{CS} = \frac{0.93 \times V_{REF\_OCP} \times N_{PS}}{6 \times I_{OUT\_OCP}} = \frac{0.93 \times 0.66V \times 6}{6 \times 5.5A} = 0.112\Omega$$

(9) Calculate maximum primary peak current:

$$I_{PPK\_MAX} = \frac{V_{CS\_LIMIT}}{R_{CS}} = \frac{0.50V}{0.112\Omega} = 4.46A$$

(10) Determine: B_{MAX} = 0.36T

(11) Calculate primary winding Lp:

$$N_P = \frac{L_P \times I_{PPK\_MAX}}{B_{MAX} \times A_E} = \frac{Lp \times 4.46A}{0.36T \times 62mm^2} = 36ts, \quad \text{Then Lp=180uH.}$$

(12) Calculate auxiliary winding turns N_{AUX}: V_{OUT_MIN} = 4.5V

$$9V < \frac{V_{OUT\_MIN}}{N_S} \times N_{AUX} \qquad 12ts < N_{AUX}$$

Calculate auxiliary winding turns: V_{OUT_MAX} = 21V

$$\frac{V_{OUT\_MAX}}{N_S} \times N_{AUX} < 120V \qquad N_{AUXH} < 34ts$$

One AUX winding is enough. AUX turns can be 12ts.

4. Secondary diode selection

(a) Maximum reverse voltage calculation:

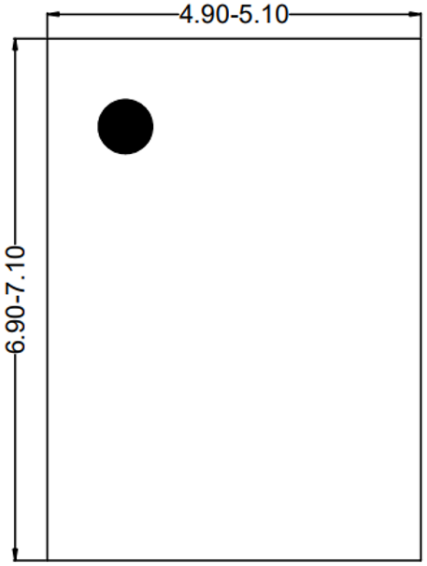
$V_{D\_R\_MAX}$ = 1.414 * V_{IN_MAX} / N_{PS} + V_{O_OVP} = 373V / 6 + 20V = 82V.

Considering the voltage spike, reverse voltage rating is recommended to be 100V.

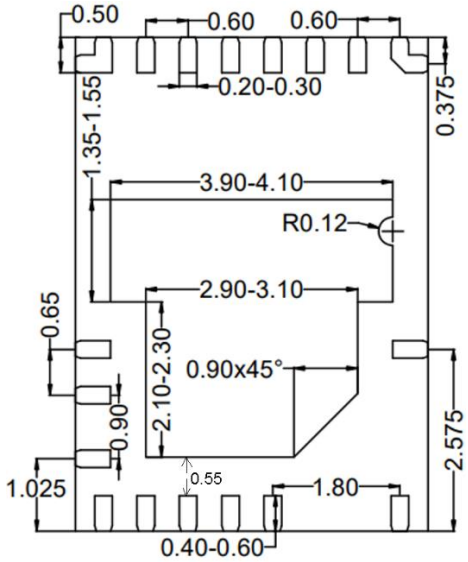
(b) Maximum instantaneous forward current:

$$I_{SPK\_MAX} = I_{PPK\_MAX} \times N_{PS} = 4.46A \times 6 = 26.8A$$

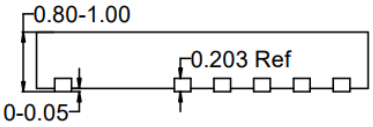
QFN5*7-18 Package Outline Drawing



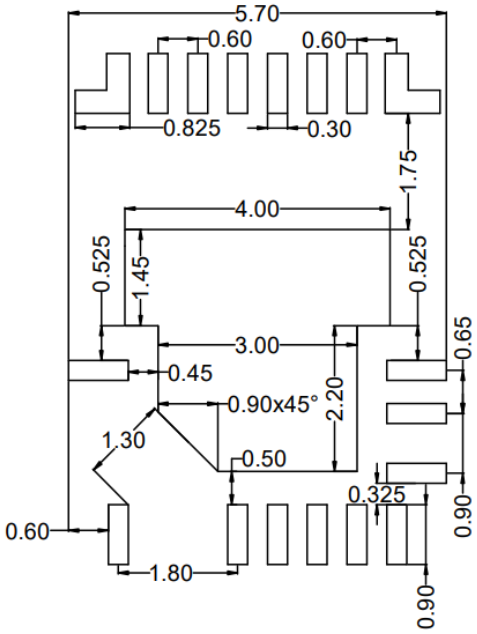
Top view



Bottmom view



Side view

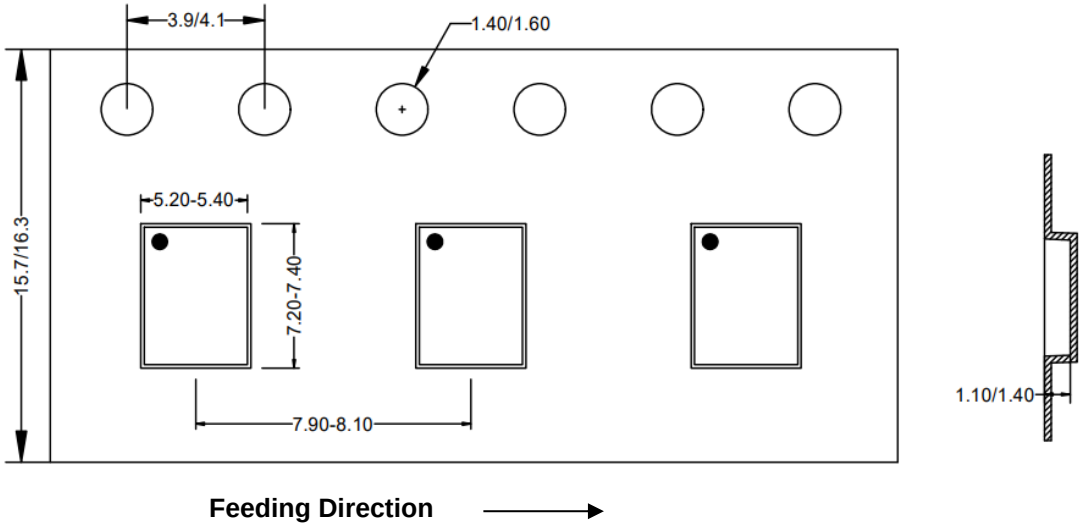


Recommended PCB layout
(Reference only)

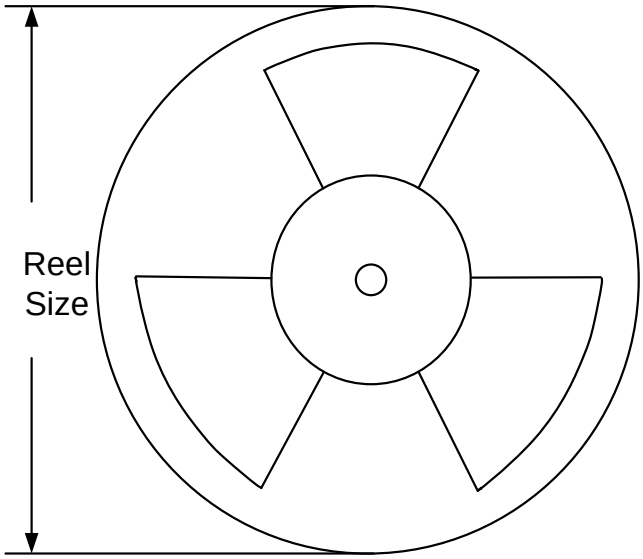
Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Tape and Reel Specification

1. Tape Orientation



2. Carrier Tape and Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
QFN5x7-18	16	8	13"	400	400	3000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
November 11，2025	Revision 1.0	Initial Release

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