Data Sheet SY22401H

Reinforced Digital Isolator

General Description

The SY22401H is a digital isolator for digital applications with 9000V_{RMS} isolation rating per UL1577, targeted for cost-sensitive applications. The device has reinforced isolation ratings according to VDE, CSA, TUV and IEC standards

Each isolation channel has a logic input and output buffer separated by double capacitive silicon dioxide (SiO_2) insulation barrier. The SY22401H has four isolation channels with three channels oriented in one direction and one isolation channel in the opposite direction, as required, for example, for isolating the signals of an SPI bus. The SY22401H includes data integrity check with fail-safe states. In the event of input power or signal loss, the default output is a logic high. See the Theory of Operation sections for further details. When used in conjunction with isolated power supplies, the SY22401H prevents high common-mode voltages present on general digital signals or an SPI data bus from damaging sensitive circuitry.

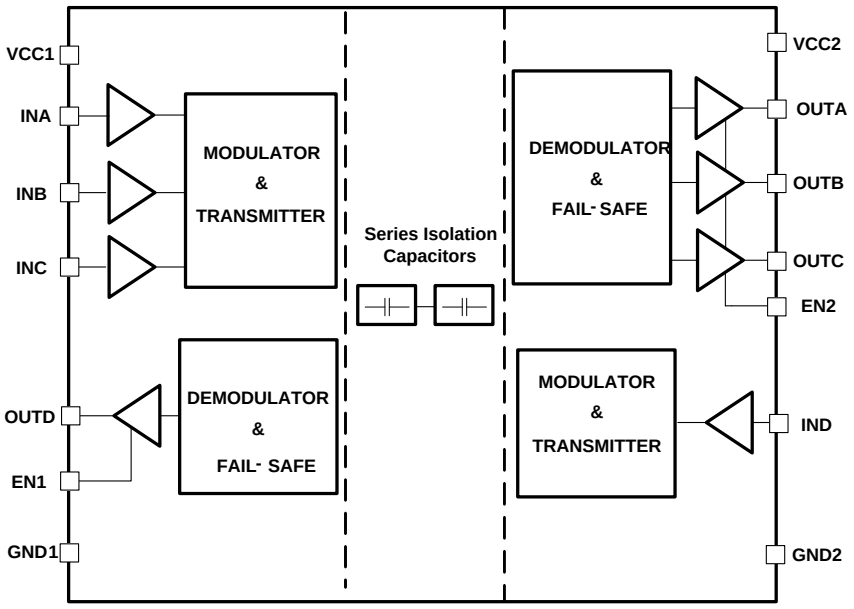
The SY22401H is available in a 16-pin SOP wide-body package.

Features

- Reinforced Isolation
- 4 channels (3 inputs + 1 output)
- 6Mbps data rate
- High CMTI: 160kV/μs (typical)
- Fail-Safe Outputs
- UL recognition(pending): 9000V for 1 minute (UL1577)
- CSA Component Acceptance Notice 5A (pending)
- VDE certificate of conformity (DIN VDE 0884-11: 2017-01, pending)
- IEC 60664-1 (pending)
- Pin-compatible with TI ISO6441

Applications

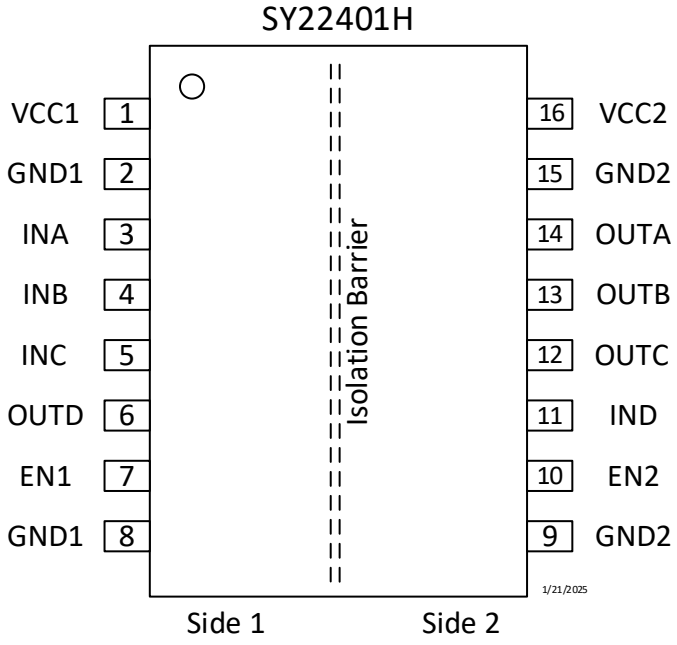
- General-Purpose Digital Isolation
- Factory Automation
- Motor Control
- Test and Measurement
- Communications
- Industrial Equipment



Ordering Information

Ordering Number	Carrier Type	Fail-Safe Output State	Temperature Range	Package
SY22401HQP	Tape & Reel	High	-40°C to +125°C	SOP-16 (Wide Body)

Pin-Out Diagram



Pin Description

Pin Number	Name	Function
1	VCC1	Positive supply
2	GND1	Ground
3	INA	Signal A input
4	INB	Signal B input
5	INC	Signal C input
6	OUTD	Signal D output
7	EN1	Output enable
8	GND1	Ground

Pin Number	Name	Function
9	GND2	Positive supply
10	EN2	Output enable
11	IND	Signal D input
12	OUTC	Signal C output
13	OUTB	Signal B output
14	OUTA	Signal A output
15	GND2	Ground
16	VCC2	Positive supply

EN1 and EN2: These pins, when de-asserted, immediately force the associated outputs to HIGH-Z state and disable the receiving amplifiers. When the voltage at the ENn pins rises, the part enters its power up sequence during which the receiving amplifiers settle before the signal outputs are enabled.

Absolute Maximum Ratings

Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation at these or other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to these Absolute Maximum Rated conditions for extended periods may affect device reliability.

	Min	Max	Unit
Supply and GND Pins			
VCC1, VCC2	2.7	5.5	V
GND1, GND2	-0.1V	+0.1V	V
Digital Input Pins			
INA, INB, INC, IND, EN1, EN2	-0.5	VCCn+0.5	V
Digital Output Pins			
OUTA, OUTB, OUTC, OUTD	-0.5	VCCn+0.5	V
Temperature Ratings			
Operating junction temperature, continuous		+125	°C
Storage temperature	-40	+165	°C
Solder temperature, 10s duration		+260	°C
ESD Rating, Human body model (HBM), per ANSI/ ESDA/JEDEC JS-001, all pins		1.5	kV
ESD Rating, Charged device model (CDM), per JEDEC specification JESD22-C101		1	kV

Thermal Ratings

Parameter	Value	Unit
Θ_{JA} Junction-to-Ambient Thermal Resistance	55.56	$\frac{°C}{W}$
Θ_{JC} Junction-to-Case (bottom) Thermal Resistance	13.75	

Recommended Operating Conditions

Parameter	Conditions	Min.	Max.	Unit
Supply Voltage		2.7	5.5	V
Operating Temperature	All modes	-40	+125 †	°C

† junction temperature is not to exceed its maximum rating

Recommended External Components

Name	From Pin	To Pin	Function	Value	Unit
C1	VCC1	GND1	Bypass capacitor	1.1 †	µF
C2	VCC2	GND2	Bypass capacitor	1.1 †	µF

† Bypass capacitors shall contain at least one 10pF, one 1nF, and one 1µF capacitor

Isolation Ratings

Symbol	Parameter	Status	Value	Unit
UL1577 †				
V_{ISO}	Withstand isolation voltage (Vrms)	In progress	9	kV
V_{ISO}	Withstand isolation voltage (Vrms)	Per Silergy lab test	9	kV
DIN VDE 0884-11 †				
IEC-60664-1 †				

† in progress

Electrical Characteristics

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit
	Digital Input Levels						
Digital low-level input Voltage		V_{IL}	VCCn = 2.7V to 5.5V			VCCn*0.25	V
Digital high-level input Voltage		V_{IH}	VCCn = 2.7V to 5.5V	VCCn*0.75			V
	Digital Output Levels						
Digital low-level out-put voltage		V_{OL}	I_{OUT} = 5mA			0.4	V
Digital high-level out-put voltage		V_{OH}	I_{OUT} = 5mA	VCCn - 0.6			V
Voltage hysteresis			VCCn = 2.7V to 5.5V	200	600	1100	mV
	Supply Current						
VCC1 current		I_{VCC1}	VCC1 = 2.7V	6	10	14	mA
VCC1 current		I_{VCC1}	VCC1 = 5.5V	6	10	14	mA
VCC2 current		I_{VCC2}	VCC2 = 2.7V	6	10	14	mA
VCC2 current		I_{VCC2}	VCC2 = 5.5V	6	10	14	mA

General Timing Specifications

Parameter	Condition	Min	Typ	Max	Unit
INC to OUTC delay (INC/OUTC use the fastest channel) †	TA=-40°C to +125°C, CL=10pF VCCn = 2.7V VCCn = 3.3V VCCn = 5.5V		 36 35 33	 40 38 35	ns
INA/OUTA delay, INC active † In this case, the INA edge was outside the INC capture region	TA=-40°C to +125°C, CL=10pF VCCn = 2.7V VCCn = 3.3V VCCn = 5.0V			 82 80 77	ns
INA/OUTA delay, INC inactive † In this case, there is no INC edge to interrupt the INA transfer	TA=-40°C to +125°C, CL=10pF VCCn = 2.7V VCCn = 3.3V VCCn = 5.0V			 70 68 65	ns
INB/OUTB delay, INC active † In this case, the INB edge was outside the INC capture region	TA=-40°C to +125°C, CL=10pF VCCn = 2.7V VCCn = 3.3V VCCn = 5.0V			 82 80 77	ns
INB/OUTB delay, INC inactive † In this case, there is no INC edge to interrupt the INB transfer	TA=-40°C to +125°C, CL=10pF VCCn = 2.7V VCCn = 3.3V VCCn = 5.0V			 70 68 65	ns
IND/OUTD delay †	TA=-40°C to +125°C, CL=10pF VCCn = 2.7V VCCn = 3.3V VCCn = 5.0V		 26 26 23	 30 28 25	ns
Data rate †				6	Mb/s
Common-mode transient immunity (CMTI) †			160		kV/µs

† Not tested in production, guaranteed by design

Timing Specifications for Synchronized Signals

Parameter	Condition	Min	Typ	Max	Unit
INC capture region around INC edge †	See INA and INB specifications	-14		+14	ns
INC/OUTA delay † When INA edge is within INC Capture Region.	TA=-40°C to +125°C, CL=10pF VCCn = 2.7V VCCn = 3.3V VCCn = 5.5V		 52 51 49	 56 54 51	ns
INC/OUTB delay † When INB edge is within INC Capture Region.	TA=-40°C to +125°C, CL=10pF VCCn = 2.7V VCCn = 3.3V VCCn = 5.0V		 52 51 49	 56 54 51	ns

Theory of Operation

The input signals (INA, INB, INC) shown on the left side of the block diagram are acquired through a Schmitt-trigger input. The detected signal is then modulated and transmitted over an isolation barrier that is implemented with a pair of on-chip differential capacitors to the opposite receiver (right side). The information transmitted via the capacitors is secured with parity and framing information that enables the receiver to detect errors.

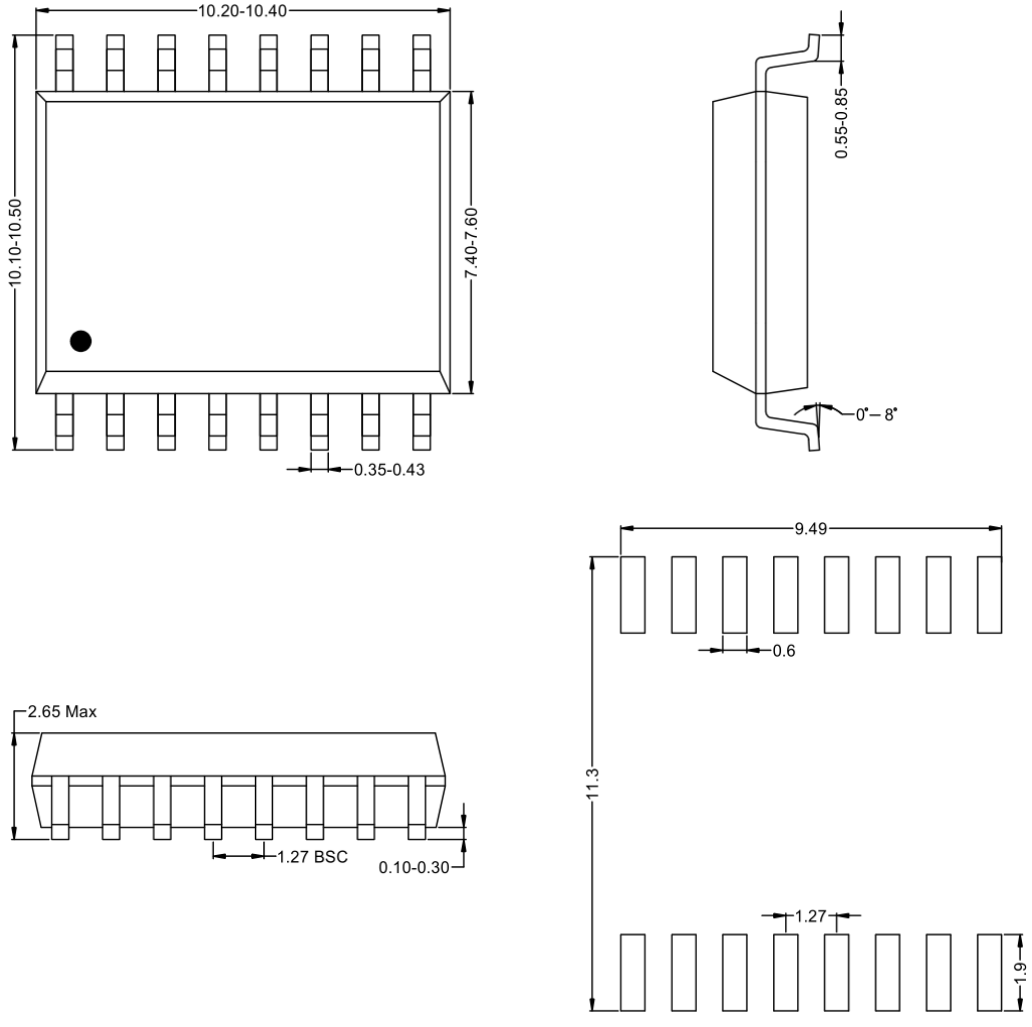
On the receiving side, the modulated signal is acquired through a dedicated comparator. The signal is then demodulated, checked for integrity, and used to drive the corresponding digital outputs (OUTA, OUTB, and OUTC).

The input signal from the right side (IND) is processed in similar fashion, just in the opposite direction, and drives the output pin OUTD.

A failsafe logic allows the digital output to be set to a predefined state (i.e., logic 1), in case an error is detected by the receiver.

The EN1 and EN2 inputs are used to enable the corresponding outputs. When pulled high, EN1 enables the output pin OUTD, and EN2 enables the output pins OUTA, OUTB, and OUTC.

Package Drawing and PCB Footprint



Note: All dimensions are in millimeters (mm) and they exclude mold flash and metal burr.

Contact Information

For more information about the SY22401H, contact support.em@silergy.com

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
1.0	1/21/2025	First release	--

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