SY20311

High Efficiency 1.5MHz, Dual 1A Synchronous Step Down Regulator

General Description

The SY20311 is a dual output, high efficiency 1.5MHz synchronous step down DC/DC regulator capable of delivering up to 1A output current for each output channel. The SY20311 operates over a wide input voltage range from 2.5V to 5.5V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

Ordering Information

SY20311□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY20311AIC	TSOT23-8	--

Features

- 2.5V to 5.5V Input Voltage
- 1.5MHz Switching Frequency
- 180° Out of Phase Operation
- Output Current: 1A per Channel
- Quiescent Current: Typical 55μA for both Channels
- Low $R_{DS(ON)}$ for Internal Switches (PFET/NFET): 260mΩ/180mΩ
- Internal Soft-start
- 100% Dropout Operation
- RoHS Compliant and Halogen Free
- Compact Package: TSOT23-8

Applications

- SSD
- Cell Phones
- Digital Cameras
- PDAs
- Portable Media Players

Typical Applications

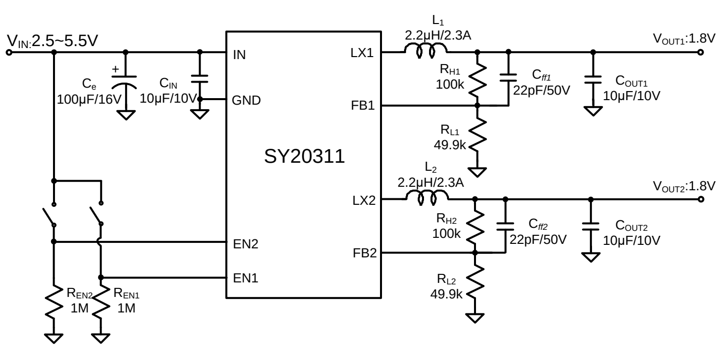


Figure 1. Schematic Diagram

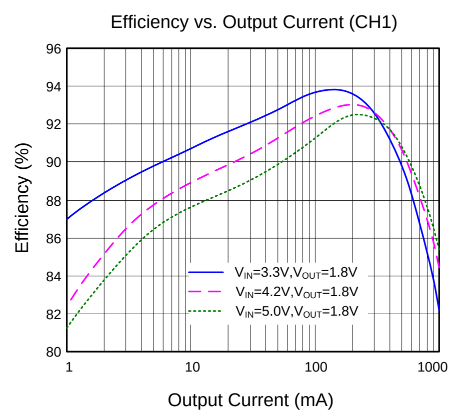
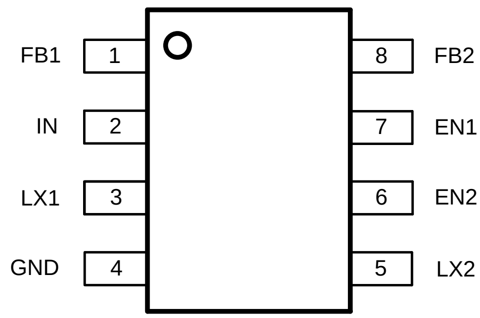


Figure 2. Efficiency vs. Output Current

Pinout (top view)



(TSOT23-8)

Top Mark: Nb*xyz* (Device code: Nb, ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin Number	Pin Description
FB1	1	Feedback pin for channel1. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage of channel 1: V_{OUT1}=0.6V× (1+R_{H1}/R_{L1})
IN	2	Power input pin. Decouple this pin to ground pin with at least a 10μF ceramic capacitor.
LX1	3	Inductor pin for output1. Connect this pin to the switching node of inductor.
GND	4	Ground pin.
LX2	5	Inductor pin for channel 2. Connect this pin to the switching node of inductor.
EN2	6	Enable pin for channel 2. Do not leave it floating.
EN1	7	Enable pin for channel 1. Do not leave it floating.
FB2	8	Feedback pin for channel2. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage of channel 2: V_{OUT2}=0.6V× (1+R_{H2}/R_{L2})

Function Block

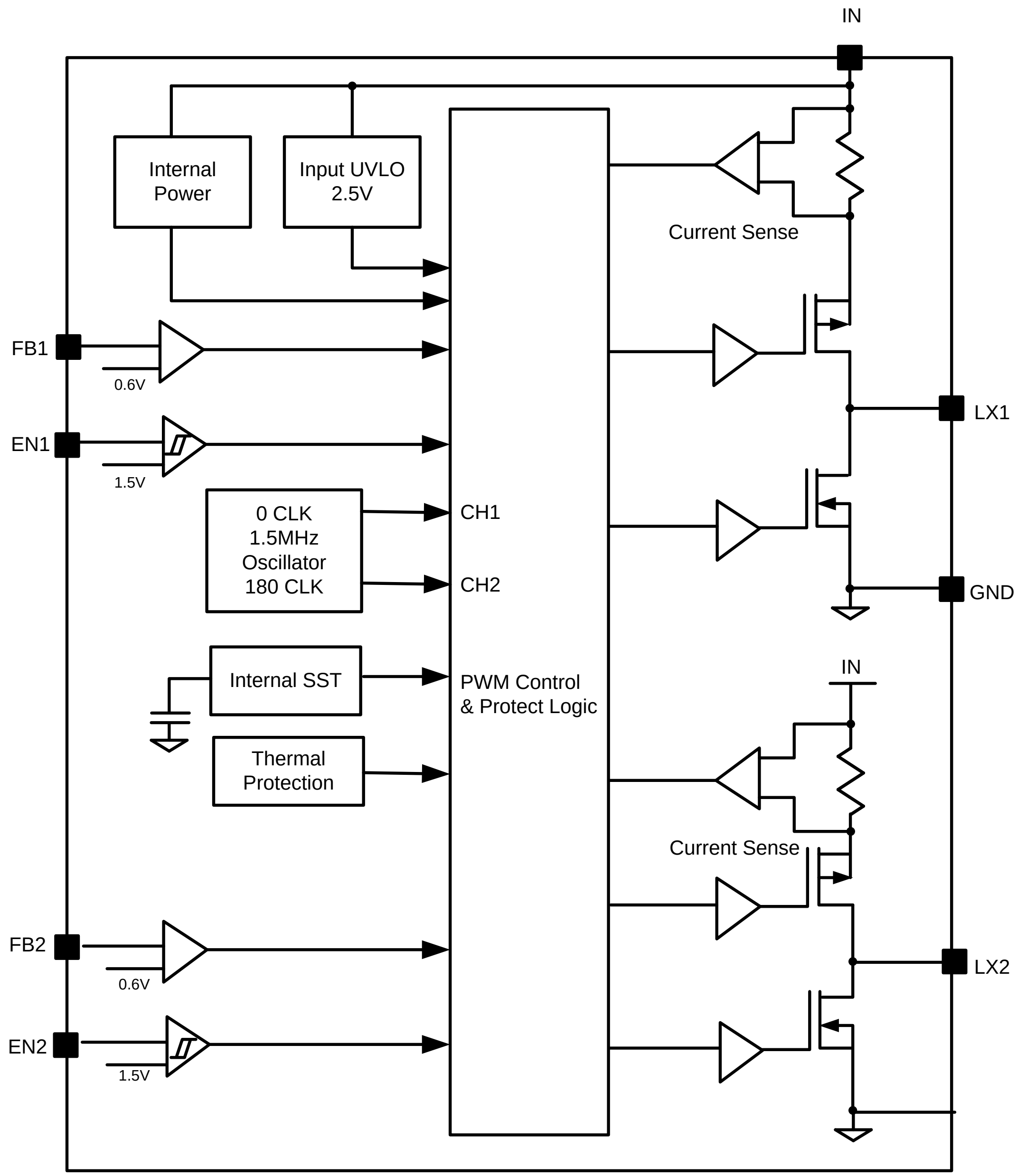


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage -- -0.3V to 6V
EN1,EN2, FB1,FB2 Voltage --- -0.3V to V_{IN}+0.6V
LX1, LX2 Voltage --- -0.3V (*1) to 6V (*2)
Power Dissipation, P_D @ T_A = 25°C TSOT23-8 --- 1.8W
Package Thermal Resistance (Note 2)

θ_{JA} --- 55°C/W

θ_{JC} --- 8°C/W

Junction Temperature Range --- 150°C
Lead Temperature (Soldering, 10 sec.) --- 260°C
Storage Temperature Range --- -65°C to 150°C

(*1) LX1, LX2 voltage tested down to -3V< 20ns
(*2) LX1, LX2 voltage tested up to +7V< 20ns

Recommended Operating Conditions (Note 3)

Supply Input Voltage -- 2.5V to 5.5V
EN1, EN2, FB1, FB2 Voltage --- V_{IN}+0.3V
Junction Temperature Range -- -40°C to 125°C
Ambient Temperature Range -- -40°C to 85°C

Electrical Characteristics

(V_{IN}= 5V, V_{OUT1}=V_{OUT2}=2.5V, L_1=L_2=2.2μH, C_{OUT1}=C_{OUT2}=10μF, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.5		5.5	V
Shutdown Current	I_{SHDN}	EN1=EN2=0		0.1	1	μA
Quiescent Current	I_Q	EN1=1 or EN2=1, I_{OUT1}= I_{OUT1}=0, no switching		45		μA
		EN1=1 and EN2=1, I_{OUT1}= I_{OUT2}=0, no switching		55		μA
Input UVLO Threshold	V_{UVLO}				2.45	V
UVLO Hysteresis	V_{HYS}			0.2		V
Oscillator Frequency	F_{OSC}	PWM operation		1.5		MHz
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C
Feedback Reference Voltage	V_{REF1}, V_{REF2}		0.588	0.600	0.612	V
PFET R_{ON}	$R_{DS(ON),P1}$ $R_{DS(ON),P2}$			260		mΩ
NFET R_{ON}	$R_{DS(ON),N1}$ $R_{DS(ON),N2}$			180		mΩ
PFET Current Limit	I_{LIM1}, I_{LIM2}		1.35			A
EN Rising Threshold	V_{ENH1}, V_{ENH2}		1.2			V
EN Falling Threshold	V_{ENL1}, V_{ENL2}				0.4	V
Output Discharge Switch On Resistance	R_{DISCH1},R_{DISCH2}			35		Ω
PFET Min On time	t_{ON}			80		ns
Internal Soft-start Time	t_{SS1}, t_{SS2}			1		ms

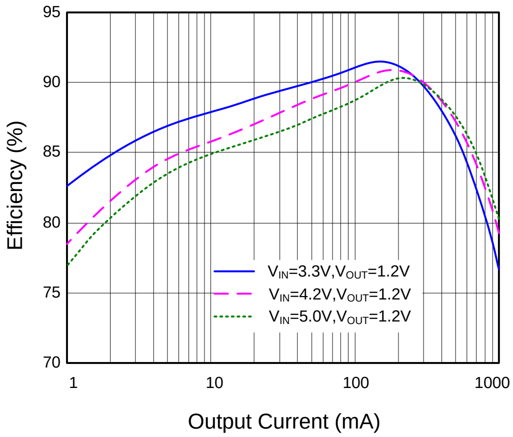
Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note2: Package thermal resistance of SY20311AIC is measured in the natural convection at T_A = 25°C on a four-layer Silergy evaluation board.

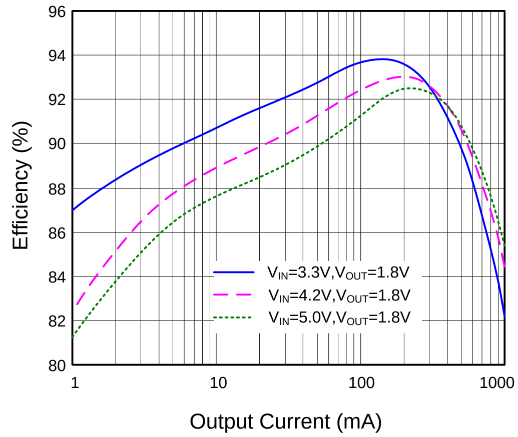
Note 3: The device is not guaranteed to function outside its operating conditions

Typical Performance Characteristics (CH1)

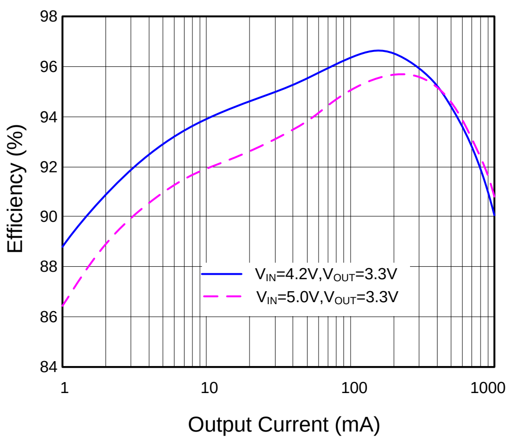
Efficiency vs. Output Current



Efficiency vs. Output Current

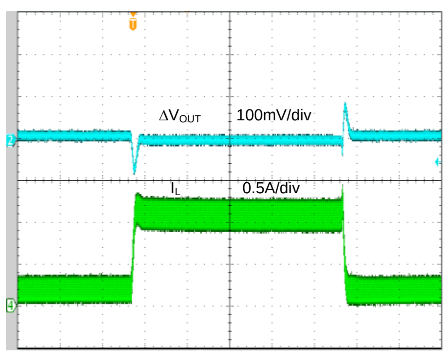


Efficiency vs. Output Current



Load Transient

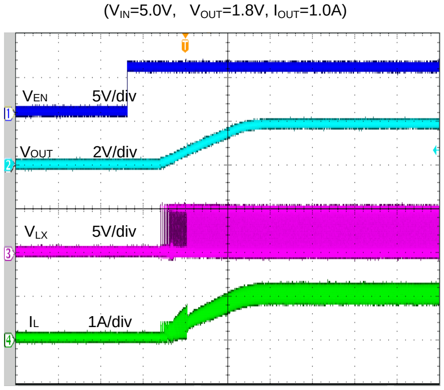
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0.1~1A)



Time (100μs/div)

Startup from Enable

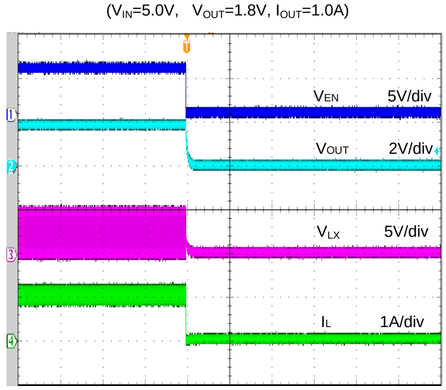
(V_{IN}=5.0V, V_{OUT}=1.8V, I_{OUT}=1.0A)



Time (400μs/div)

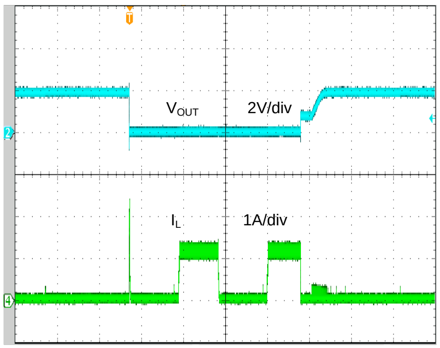
Shutdown from Enable

(V_{IN}=5.0V, V_{OUT}=1.8V, I_{OUT}=1.0A)



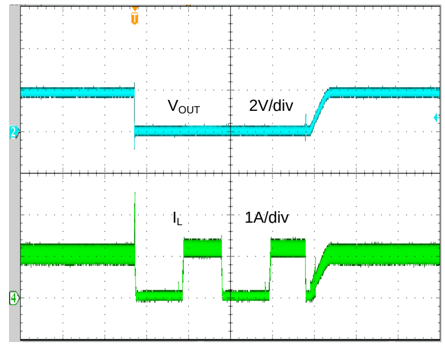
Time (400μs/div)

Short Circuit Protection
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0A ~ short)



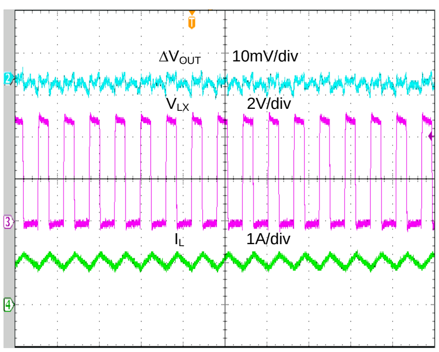
Time (2ms/div)

Short Circuit Protection
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=1A ~ short)



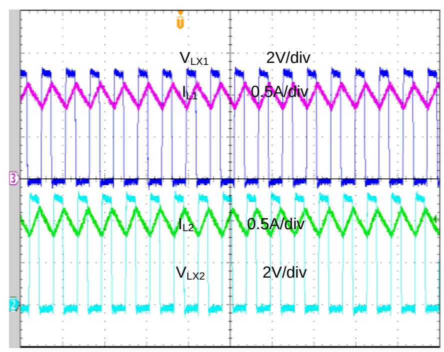
Time (2ms/div)

Output Ripple
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=1.0A)



Time (1μs/div)

180° Out of Phase
(V_{IN}=5.0V,V_{OUT1}=1.8V,I_{OUT1}=1.0A,V_{OUT2}=1.8V,I_{OUT2}=1.0A)



Time (1μs/div)

Operation

The SY20311 is a dual output, high efficiency 1.5MHz synchronous step down DC/DC regulator capable of delivering up to 1A output current for each output channel. The SY20311 operates over a wide input voltage range from 2.5V to 5.5V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

Applications Information

Because of the high integration in the SY20311, the application circuit based on this IC is rather simple. Only the input capacitor C_{IN}, the output capacitor C_{OUT}, the output inductor L and the feedback resistors (R_H and R_L) need to be selected for the targeted applications.

Feedback Resistor Divider R_H and R_L

Choose R_H and R_L to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R_H and R_L. A value between 100k and 1M is highly recommended for both resistors. If R_L=120k is chosen, then R_H can be calculated to be:

$$R_H = \frac{(V_{OUT} - 0.6V) \times R_L}{0.6V}$$

Input Capacitor C_{IN}

The ripple current through the input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1-D)}$$

This formula has a maximum in $V_{IN}=2V_{OUT}$ condition, where $I_{CIN\_RMS}=I_{OUT}/2$. This simple worst-case condition is commonly used for DC/DC design.

With the maximum load current of 1.0A, a typical X5R or better grade ceramic capacitor with 10V rating and larger than 10μF capacitance can handle this ripple current well. To minimize the potential noise problem, ceramic capacitor should be placed really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirement. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use a X5R or better grade ceramic capacitor with 10V rating and greater than 10μF capacitance.

Output Inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where Fsw is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY20311 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load condition.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mΩ to achieve a good overall efficiency.

Load Transient Considerations

The SY20311 integrates the compensation components to achieve good stability and fast transient responses. In some application, adding a ceramic capacitor (feed-forward capacitor, C_{ff}) in parallel with R_H may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements. Typically， for 1.2V/1.8V/3.3V output, the R_H, R_L, C_{ff} is recommended as below:

Table1. Recommended Component Selection

V_{OUT}	R_H	R_L	C_{ff}
1.2V	50k	50k	22pF
1.8V	100k	49.9k	22pF
3.3V	100k	22.1k	47pF

Layout Design

The layout design of SY20311 is relatively simple. For the best efficiency and minimum noise problem, the following components should be placed close to the IC: C_{IN}, L, R_H and R_L.

1) It is desirable to maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance. If the board space allows, a ground plane is highly desirable. Reasonable vias are suggested to be placed underneath the ground pad to enhance the soldering quality and thermal performance.

2) Input capacitor must be close to the IN and GND pins. The loop area formed by input capacitor, IN and GND pins must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem. For the smallest loop area of C_{IN}, IN and GND, LX1 pin copper can pour area on internal or bottom layer.

4) The components R_H and R_L and the trace connecting to the FB pin must NOT be adjacent to the LX node on the PCB layout to avoid the noise problem.

5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1MΩ resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

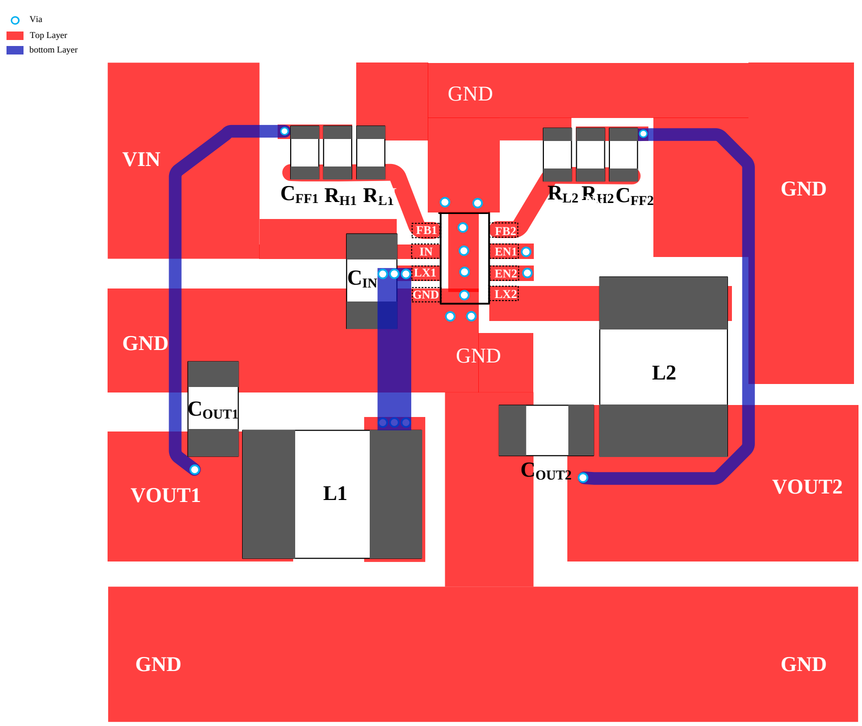
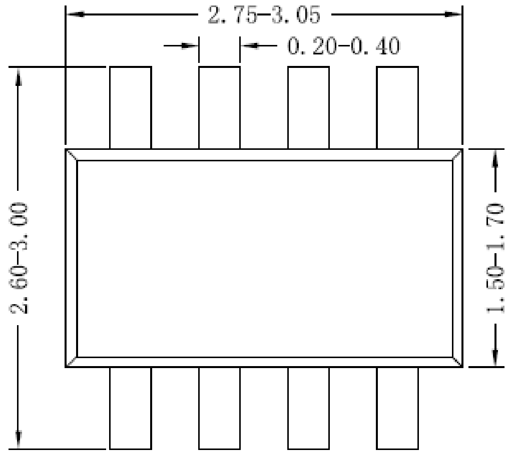
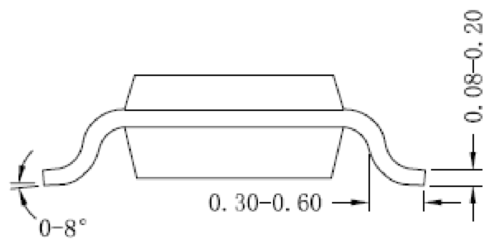


Figure4. PCB Layout Suggestion

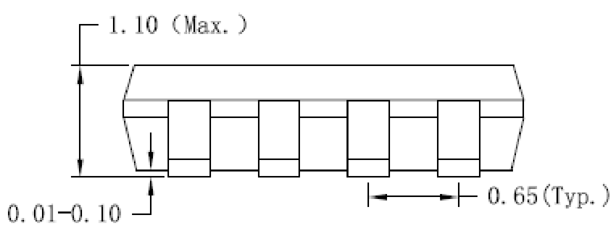
TSOT23-8 Package Outline Drawing



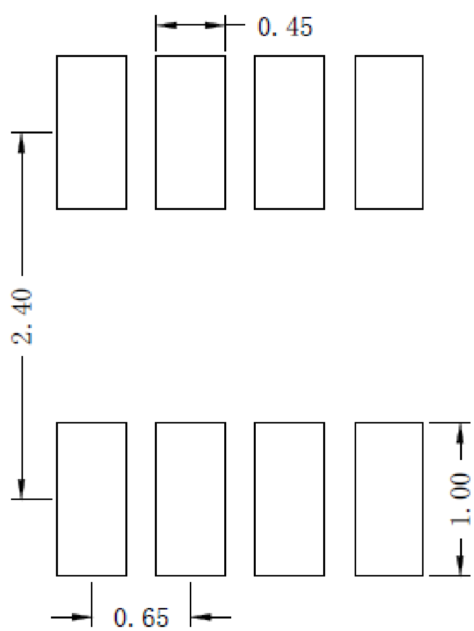
Top view



Side view A



Side view B



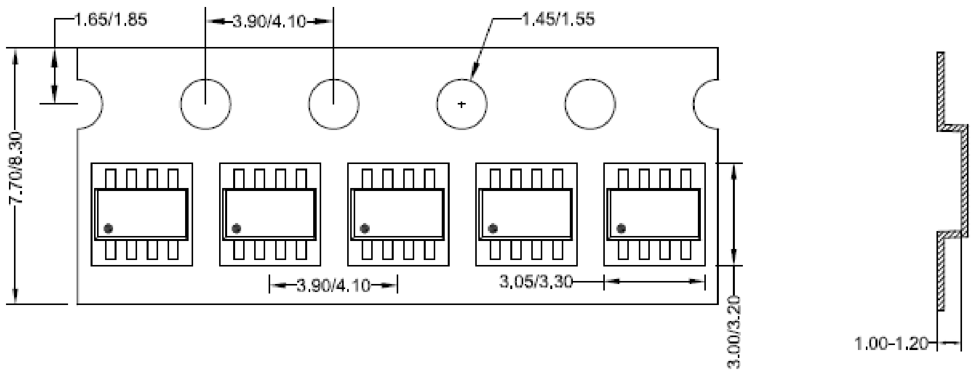
Recommended PCB layout
(Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr

Taping & Reel Specification

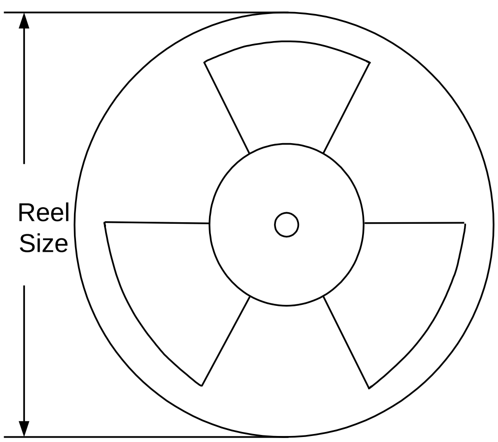
1. Taping orientation

TSOT23-8



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
TSOT23-8	8	4	7	400	160	3000

3. Others: NA

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