SQ33607

IEEE 802.3af/at Compliant PoE PD Interface with High Efficiency PSR/SSR Flyback Controller

General Description

The SQ33607 is a fully integrated IEEE 802.3 af/at PoE compliant Powered Device (PD) power supply controller. It includes the PD interface and a high efficiency PSR/SSR Flyback controller.

The PD interface has all the functions to comply with IEEE 802.3af/at, including detection, 1-event and 2-event classification, ~100mA inrush current limit, 900mA operation current limit, auto maintain power signature (AMPS), as well as 100V rated Hot-swap MOSFET. The PD interface also supports Auxiliary Adaptor Oring and type-2 indicator.

The PWM controller is specifically optimized for low cost, small size isolated flyaback configuration, with either primary-side regulation (PSR) or secondary-side regulation (SSR). The device integrates a high voltage start-up circuit, using current mode, quasi constant-frequency control to avoid sub-harmonic oscillations and no need of slope compensation.

SQ33607 is available in a QFN 4mm x 4mm -20 pin package.

Features

- Fully Compatible with 802.3af/at Specifications
- 100V 0.45Ω PD Integrated Pass Switch
- 30W maximum power
- 100mA PD Inrush Current limit
- 900mA PD Normal Operation Current Limit
- Auxiliary Adaptor ORing Support
- Flexible Topology:
  - ➢ Primary-Side Regulated (PSR) Flyback (250kHz/400kHz Selectable)
  - ➢ Secondary-Side Regulated (SSR) Flyback (Programmable Frequency)
- Output Diode Compensation in PSR Mode
- Cycle-by-Cycle Current Sense Limit
- Precision Voltage Reference
- Frequency Modulation for EMI reduction
- Programmable Soft-start
- OLP Compensation for Wide-Input Range
- Externally Programmable Thermal Shutdown
- Programmable Line Under Voltage Lockout (UVLO) with Adjustable Hysteresis
- Hiccup Protection for OLP, SCP, OVP and Thermal Shutdown

Applications

- IEEE 802.3af/at-Compliant Devices
- Security Cameras
- Video Telephones
- WLAN Access Points
- IoT Devices

Typical Application

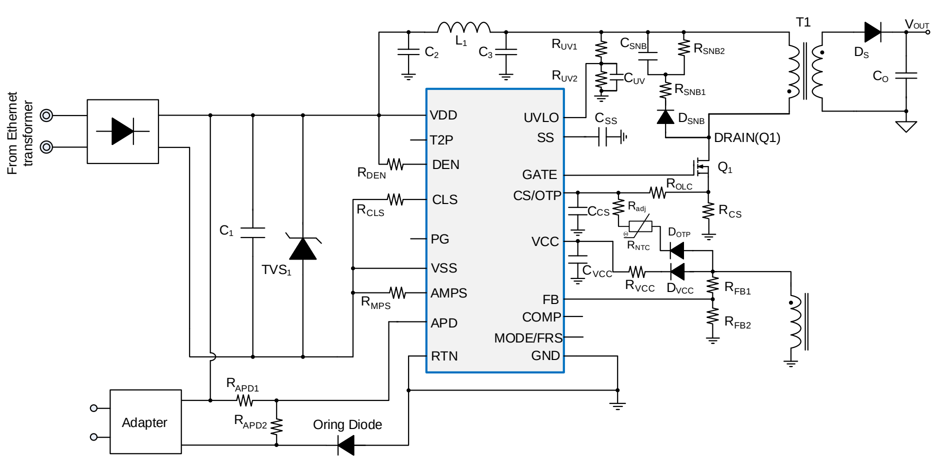


Fig.1 Typical Application-Isolated PSR Flyback Converter

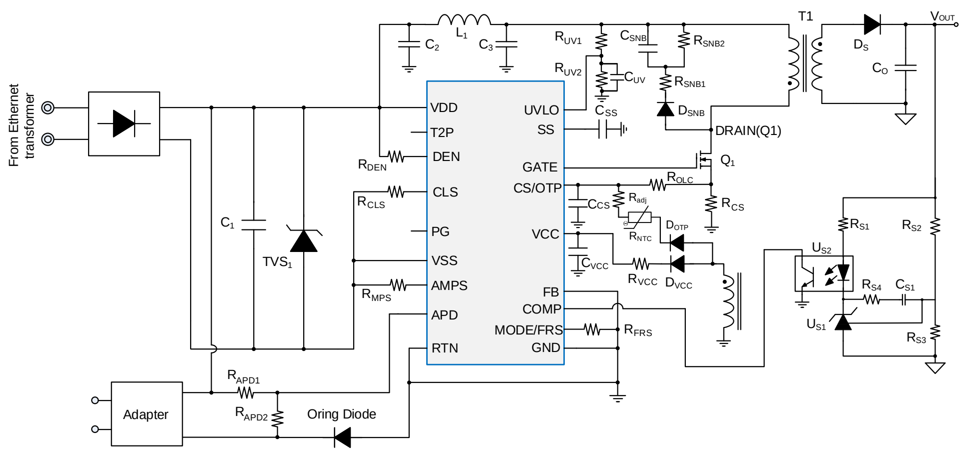


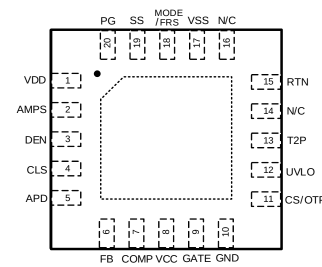
Fig.2 Typical Application-Isolated SSR Flyback Converter

Ordering Information

Ordering Part Number	Package type	Top Mark
SQ33607QYQ	QFN4×4-20 RoHS-Compliant and Halogen-Free	**FNA*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	VDD	Positive power supply terminal for PoE and controller input power rail.
2	AMPS	Automatic MPS control. Connect a resistor with appropriate power rating (to support the MPS current) from AMPS to VSS to program the MPS current amplitude. Leave AMPS open if not used.
3	DEN	Detection. Connect a 24.9kΩ resistor between VDD and DEN for PoE detection.
4	CLS	Classification. Connect a resistor from CLS to VSS to program the classification current.
5	APD	Adaptor power input detector. Drive VDD-APD above 1.5V to disable hot-swap MOSFET and CLASS functions and force T2P and PG active.
6	FB	Output voltage feedback pin. Connect a resistor divider from sensing winding to regulate output voltage in PSR mode. In SSR mode, the FB should be connected to GND.
7	COMP	Loop compensation pin. Let it float in PSR mode, and internally pulled up to 3.3V through 10k resistor in SSR mode.
8	VCC	DCDC internal circuit supply pin. Connect a bypass capacitor between this pin to GND.
9	GATE	Flyback MOSFET gate driver pin.
10	GND	Flyback controller ground.
11	CS/OTP	Current sense and external over-temperature protection pin.
12	UVLO	Input undervoltage detector. The input voltage is scaled down and sampled using a resistor divider. The controller is enabled once V_{UVLO} exceeds the enable threshold.
13	T2P	Type-2 PSE indicator. T2P is an open-drain output. T2P pulled low to RTN indicates the presence of a Type-2 PSE or the presence of a wall adapter.

15	RTN	Drain of PD hot-swap MOSFET. Connect GND to RTN in PCB layout.
17	VSS	Negative power supply terminal from PoE input power rail.
18	MODE/FRS	PSR/SSR mode setting and SSR frequency setting pin. Connect a resistor from FRS to GND to program the converter switching frequency in SSR Mode.
19	SS	Soft-start setting pin. A capacitor from SS to GND pin sets the soft-start (I_{SSC} charge current) for the DC-DC converter.
20	PG	PD supply power good indicator and power down input. This signal enables the DCDC converter internally. It is pulled up by internal 3.3V voltage source; leave floating in application. Pulling PG down during operation will shut down the flyback converter, forcing sleep mode.
14,16	N/C	Not connected internally.
EP	Exposed pad	This is the thermal pad for the device and should be soldered to ta plane connected to VSS.

Block Diagram

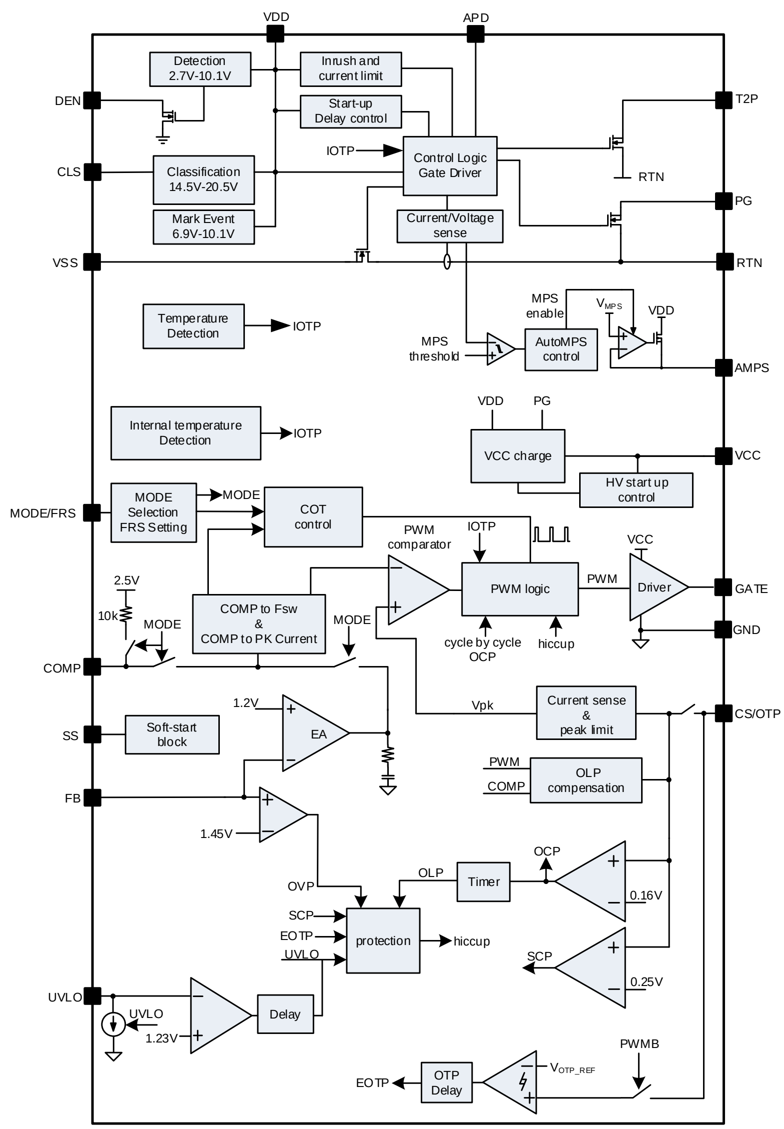


Fig.3 Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)		Min	Max	Unit
Pins Voltage Respects to VSS				
VDD, RTN, DEN, APD, T2P		-0.3	100	V
AMPS (Note 6) , CLASS (Note 6)		-0.3	5.5	V
Pins Voltage Respects to RTN(Note 7)				
VDD, T2P		-0.3	100	V
Pins Voltage Respects to GND				
VDD		-0.3	100	V
VCC, GATE		-0.3	20	V
UVLO		-0.3	16	V
FB, MODE/FRS, CS/OTP, PG		-0.3	3.3	V
SS, COMP		-0.3	3.6	V
Pins Current:				
T2P Sink Current			15	mA
PG Sink Current			0.8	mA
AMPS Source current			15	mA
Junction Temperature, Operating		-45	150	°C
Lead Temperature (Soldering, 10 sec.)			260	°C
Storage Temperature		-65	150	°C
V_{ESD} Electrostaic Discharge	Human-body model(HBM), per ANSI/ESDA/JEDEC JS-001-2023		±2000	V
	Charged-device model(CDM), per ANSI/ESDA/JEDEC JS-002-2022		±500	V

Thermal Information

Parameter (Note 2)	Min	Max	Unit
θ_{JA} Junction-to-ambient Thermal Resistance		35.5	°C/W
θ_{JC} Junction-to-case Thermal Resistance		14.1	°C/W
θ_{JB} Junction-to-Board Thermal Resistance		5.7	°C/W
P_D Power Dissipation T_A = 25°C		3.52	W

Recommended Operating Conditions

Parameter(Note 3)	Min	Max	Unit
VDD	10	57	V
VCC, GATE	8	15	V
Junction Temperature T_J	-40	125	°C

Electrical Characteristics(PD Interface Part)

(VDD, CLASS, DEN and RTN voltages are referred to VSS, T2P voltage is referred to RTN. VDD-VSS=48V, VSS=0V, R_{DEN}=24.9 kΩ, R_{CLS}=63.4 Ω, T_J=-40℃ to +125℃, typical values are tested at T_J=25℃, unless otherwise specified (Note 4.)

Parameter		Symbol	Test conditions	Min	Typ	Max	Unit
Detection	Detection on	V_{DNT_ON}	V_{DD} rising	0.8	1.1	1.4	V
	Detection off	V_{DEN_OFF}	V_{DD} rising	10.1	11	12.5	V
	DEN Leakage Current	V_{DEN_LK}	V_{DEN}=V_{DD} =57V, measure I_{DEN}		0.1	5	µA
	Bias Current	I_{BIAS}	V_{DD} =10.1V, float DEN pin, not in Mark status, measure I_{SUPPLY}			12	µA
	Detection Current	I_{DEN}	V_{DD}=1.4V, measure I_{SUPPLY}	53.8	55.6	58.3	µA
			V_{DD}=10.1V, measure I_{SUPPLY}	395	412	425	µA
Classification	V_{CLASS} Output Voltage	V_{CLASS}	13V<VDD<21V,1mA<I_{CLASS}<42mA	2.37	2.5	2.63	V
	Classification Current	I_{CLASS}	13 V ≤ V_{DD}≤ 21 V, Not tested in production, guaranteed by V_{CLASS}				
			R_{CLASS} = 1270 Ω, 13 V ≤ V_{DD}≤ 21 V		2		mA
			R_{CLASS} = 243 Ω, 13 V ≤ V_{DD}≤ 21 V		10.55		mA
			R_{CLASS} = 137 Ω, 13 V ≤ V_{DD}≤ 21 V		18.7		mA
			R_{CLASS} = 90.9 Ω, 13 V ≤ V_{DD}≤ 21 V		28.15		mA
			R_{CLASS} =63.4 Ω, 13 V ≤ V_{DD}≤ 21 V		40.4		mA
	Classification Lower Threshold	V_{CL_ON}	V_{DD} rising, Class regulator turns on	11	12	13	V
	Classification upper Threshold	V_{CL_OFF}	V_{DD} rising, Class regulator turns off	21	22	23	V
	Classification Hysteresis	V_{CL_H}	Low side hysteresis		0.9		V
			High side hysteresis		0.5		V
	Mark Event Reset Threshold	V_{MARK_L}		4	5	6	V
	Max Mark Event Voltage	V_{MARK_H}		10.2	11	11.8	V
	Mark Event Resistance	R_{MARK}	2-point measure at 7V and 10V	6	9	12	kΩ
	IC Supply Current during Classification	I_{IN_CLASS}	V_{DD}=17.5V, CLASS floating		220	280	µA
	Class Leakage Current	I_{LK}	V_{DD}=57V, V_{CLASS}=0V			2	µA
PD UVLO	VDD Turn on Threshold	V_{DD_R}	VDD rising	33.5	35	36.5	V
	VDD Turn off Threshold	V_{DD_F}	VDD falling	29	31	32	V
	VDD UVLO Hysteresis	V_{DD_HYS}			4		V
	IC Supply Current during Operation	I_{IN}		290	390	490	µA
PASS device and current limit	ON Resistance	R_{DS_RTN}	I_{RTN}=100mA，T_J=25℃		0.45	0.55	Ω
			I_{RTN}=100mA，T_J=125℃		0.65		Ω
	Leakage Current	I_{RTN_LK}	V_{DD}=V_{RTN}=57V		1	15	µA
	Current Limit	I_{LIMIT}	V_{RTN}=1 V	750	900	1050	mA
	Inrush Current Limit	I_{INRUSH}	V_{RTN}=2 V	45	110	175	mA
	Inrush Current Termination		V_{RTN} falling	1.1	1.2	1.3	V

Parameter		Symbol	Test conditions	Min	Typ	Max	Unit
PASS device and current limit	Inrush to Operation Mode Delay	T_{DELAY}		80	100	120	ms
	Current Fold-back Threshold		V_{RTN} rising	8.5	10.5	12.5	V
	Fold-back Deglitch Time		V_{RTN} rising to inrush current fold-back	0.85	1.1	1.35	ms
APD	Adaptor Detection Threshold Voltage	V_{APD_EN}	Respect to VDD	-1.3	-1.5	-1.7	V
		V_{APD_Hys}	Respect to VDD		0.5		V
AMPS	MPS DC Supply Current		Startup has completed, I_{RTN} = 0 mA			0.8	mA
	Auto MPS Pulsed Voltage		Startup has completed, I_{RTN}<29 mA, R_{MPS}≥160Ω	2.37	2.5	2.63	V
	Automatic MPS Falling Current Threshold		Startup has completed, I_{RTN} threshold to generate MPS pulses		29		mA
			Hysteresis on RTN current		3		mA
	POE MPS Time High	T_{MPS_HIGH}		85	106	125	ms
	POE MPS Time Low	T_{MPS_LOW}		170	216	265	ms

Electrical Characteristics(Flyback Controller part)

(All voltages are referred to GND. T_J=-40℃ to +125℃, typical values are tested at T_J=25℃, unless otherwise specified(Note 4).)

Parameter		Symbol	Test conditions	Min	Typ	Max	Unit
Power Supply	VCC Turn on Threshold	V_{VCC_ON}	V_{VCC} rising	6.5	7	7.5	V
	VCC min Voltage	V_{VCC_MIN}	V_{VCC} falling	5.5	6	6.5	
	VCC Turn off Threshold	V_{VCC_OFF}	V_{VCC} falling	4.5	5	5.5	
	VCC OVP Threshold	V_{VCC_OVP}	V_{VCC} rising	18	19	20	
	Quiescent Current	I_Q	PSR , f_{SW}= F_{SW_MIN}		1.25		mA
			SSR , COMP=0		1.1		
	HV Start-up Current	I_{VC}	V_{VDD}≥ 18V, V_{VCC} = 0 V	8	18		
			V_{VDD}=10V, V_{VCC}=0V	5	13		
Voltage Feedback	FB Reference Voltage	V_{REF}	T_J= 25℃	1.188	1.2	1.212	V
			T_J= -40℃ to +125℃	1.182	1.2	1.218	
	FB OVP Threshold	V_{FB_OVP}		1.35	1.45	1.55	
	FB Sample Blanking	$T_{blanking}$	PSR mode, F_{sw}=250kHz, start from PWM downward edge	390	517	645	ns
			PSR mode, F_{sw}=400kHz, start from PWM downward edge	280	365	450	
	FB Sample Period	T_{sample}	PSR mode, F_{sw}=250kHz/400kHz,	100	135	175	
COMP	COMP Open Circuit Voltage		SSR mode, float COMP		3.3		V
	COMP Internal Pull up Resistor		SSR mode		10		kΩ

Parameter		Symbol	Test conditions	Min	Typ	Max	Unit
PWM Switching (Note 8)	Switching Frequency in SSR Mode	F_{SW}	R_{FRS}=7.5k Ω	-10%	500	+10%	kHz
	Switching Frequency in PSR mode	F_{SW_PSR}	R_{MODE}=0Ω	-10%	250	+10%	kHz
			R_{MODE}=open	-10%	400	+10%	kHz
	Minimum fold-back frequency in PSR mode	F_{SW_MIN}	In PSR Mode, Internal COMP=0V		4		kHz
	Maximum ON time in PSR mode		PSR		5		us
	Maximum DUTY in SSR mode		SSR		83		%
Soft start	Soft Start Charge Current	I_{SSC}			10		µA
Gate Driver	Peak Source Current	I_{SOURCE}	V_{VCC} =10V, V_{GATE} = 0 V, pulsed measurement		0.5		A
	Peak Sink Current	I_{SINK}	V_{VCC} =10V, V_{GATE}=10 V, pulsed measurement		0.9		A
Current Sense	Maximum Current Sense Limit	V_{CS_MAX}		145	160	185	mV
	Low Threshold Current Limit	V_{CS_MIN}	In PSR mode		42.5		mV
	SCP Limit	V_{CS_SCP}		200	250	300	mV
	Current Limit Leading Edge Blanking Time, same as T_{ON-MIN}	T_{LEB}		150	200	250	ns
MODE/FRS	MODE pin detection current	I_{MODE}		31	40	49	µA
	MODE pin detection period(Note 5)	T_{MODE}			100		µs
	MODE pin detection threshold voltage	V_{MODE}	Voltage level 1 range (PSR Mode,FRS=250kHz)			0.09	V
			Voltage level 2 range (SSR Mode,Programmable FRS:100kHz~500kHz)	0.2		1.85	V
			Voltage level 3 range (PSR Mode,FRS=400kHz)	2.1			V
UVLO	UVLO Enable Threshold	V_{ENABLE}	V_{UVLO} rising		1.25		V
	UVLO Protection Threshold	V_{UVP}		1.17	1.2	1.23	V
	Pull down Current in UVLO Protection Mode	I_{UVLO_hys}	V_{UVLO} =V_{ENABLE}-0.1V	16	20	24	µA
External OTP	Over-temperature Protection Threshold	V_{OTP_REF}	V_{OTP} rising	0.96	1	1.04	V
	Over-temperature Protection Hysteresis	V_{OTP_HYS}	V_{OTP} falling		80		mV
	OTP Delay	T_{OTP_Delay}	V_{OTP}=$V_{OTP-REF}$+20mV		4		PWM cycles
Protection	Over Load Protection Hiccup on Time (Note 5)				4		ms

Parameter		Symbol	Test conditions	Min	Typ	Max	Unit
Protection	Protection Hiccup off Time(Note5)				64		ms
	Thermal Shutdown Temperature (Note5)	T_{SD}			160		℃
	Thermal Shutdown Hysteresis (Note5)	T_{HYS}			20		℃

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in natural convection at T_A = 25°C on a 1oz Four-layer Silergy evaluation board. Case temperature θ_{JC} is measured at pin 17 or pin 15.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25℃. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

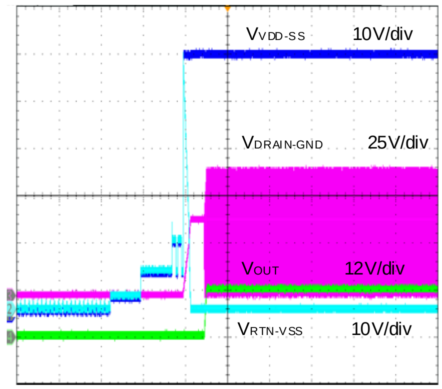
Note 5: Guaranteed by design or statistical correlation and not production tested.
Note 6: Voltage should not be externally applied to this pin.
Note 7: RTN should be connected to GND of the Flyback controller in application.
Note 8: Frequency and duty cycle are not including the range of jitter frequency.

Typical Performance Characteristics

(PSE input or 42.5V~57V DC input before the bridge rectifiers, output spec: 12Vdc/2.1A, Ambient temperature: 25±5℃.)

Start-up with at PSE Input

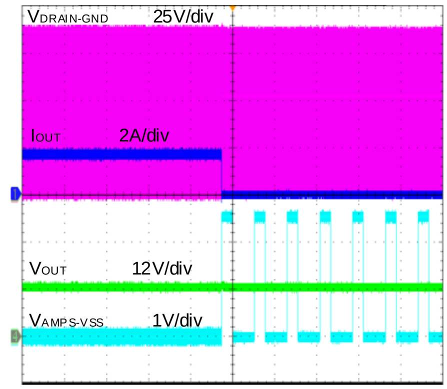
(I_O=2.1A)



Time (200ms/div)

After PSE Power Supply

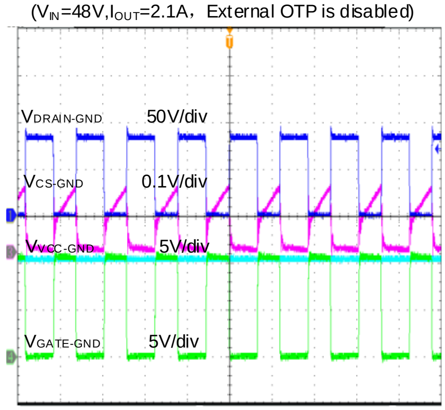
(I_{OUT}=2.1A→0A，AMPS Function is activated)



Time (400ms/div)

Steady

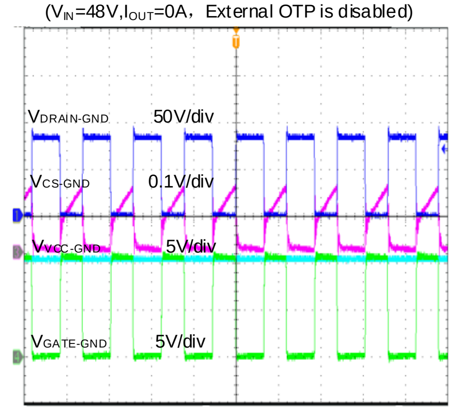
(V_{IN}=48V,I_{OUT}=2.1A，External OTP is disabled)



Time (2µs/div)

Steady

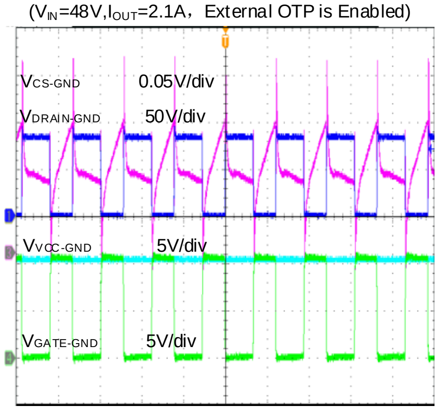
(V_{IN}=48V,I_{OUT}=0A，External OTP is disabled)



Time (1µs/div)

Steady

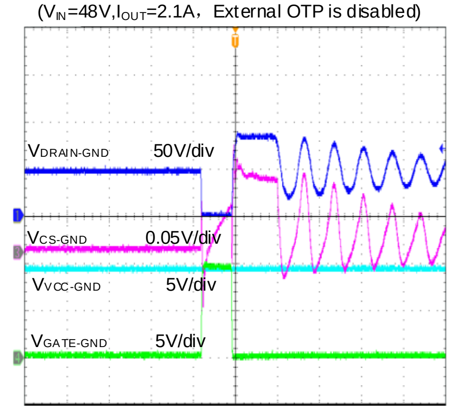
(V_{IN}=48V,I_{OUT}=2.1A，External OTP is Enabled)



Time (2µs/div)

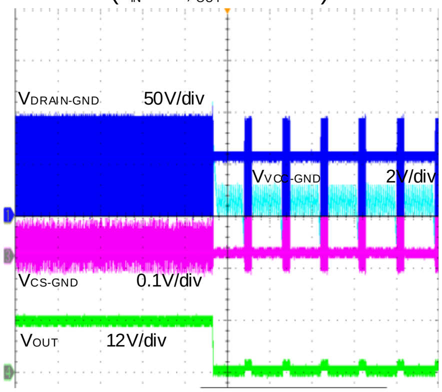
Steady

(V_{IN}=48V,I_{OUT}=2.1A，External OTP is disabled)



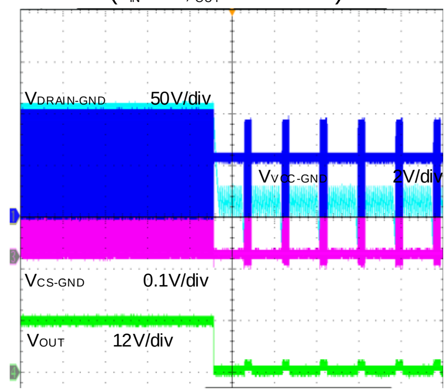
Time (1µs/div)

OLP Entry
(V_{IN}=57V,I_{OUT}=0A to short)



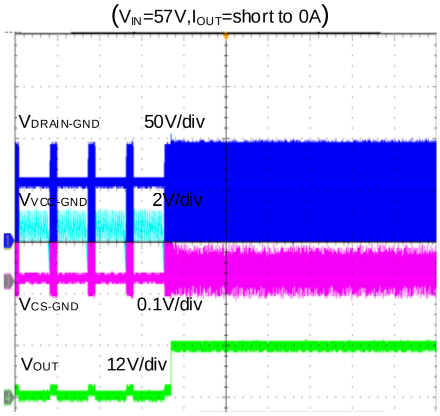
Time (100ms/div)

OLP Entry
(V_{IN}=57V,I_{OUT}=2.1A to short)



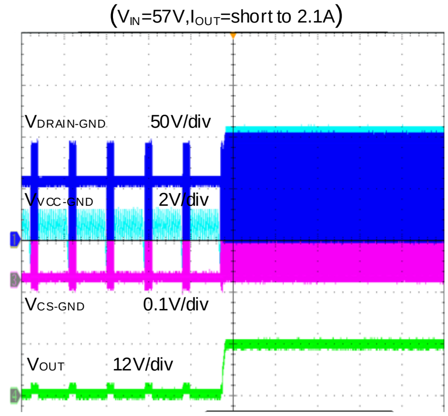
Time (100ms/div)

OLP Recovery
(V_{IN}=57V,I_{OUT}=short to 0A)



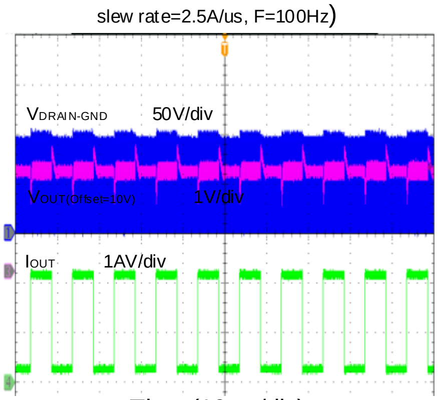
Time (100ms/div)

OLP Recovery
(V_{IN}=57V,I_{OUT}=short to 2.1A)



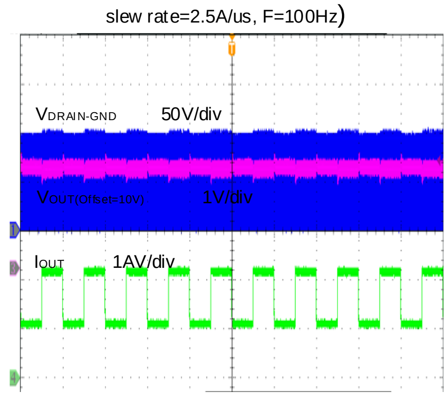
Time (100ms/div)

Load Transient
(V_{IN}=48V,I_{OUT}:0.21→2.1A,
slew rate=2.5A/us, F=100Hz)

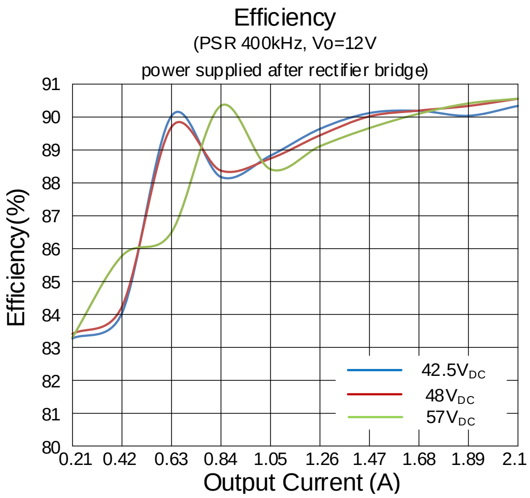


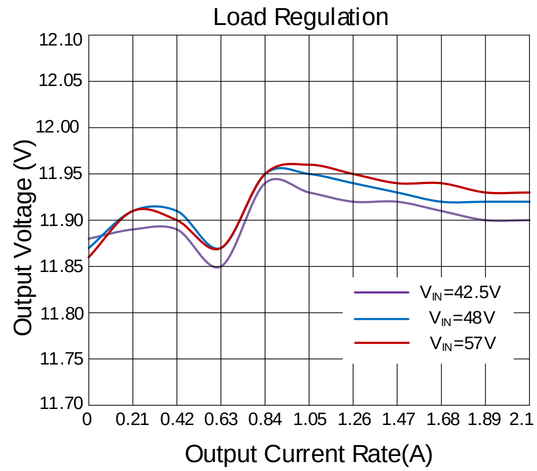
Time (10ms/div)

Load Transient
(V_{IN}=48V,I_{OUT}:0.21→1.05A,
slew rate=2.5A/us, F=100Hz)



Time (10ms/div)


Efficiency
(PSR 400kHz, Vo=12V
power supplied after rectifier bridge)
Efficiency(%)
Output Current (A)
42.5VDC
48VDC
57VDC
91
90
89
88
87
86
85
84
83
82
81
80
0.21 0.42 0.63 0.84 1.05 1.26 1.47 1.68 1.89 2.1


Load Regulation
Output Voltage (V)
Output Current Rate(A)
VIN=42.5V
VIN=48V
VIN=57V
12.10
12.05
12.00
11.95
11.90
11.85
11.80
11.75
11.70
0 0.21 0.42 0.63 0.84 1.05 1.26 1.47 1.68 1.89 2.1

Detailed Description

General Features

Overview

The IEEE 802.3at standard establishes a higher power allocation for Power over Ethernet (PoE) than IEEE 802.3af. Power sourcing equipment (PSE) and power devices (PD) are distinguished as Type-1 (compliant with IEEE 802.3af power levels) or Type-2 (compliant with IEEE 802.3at power levels). The IEEE 802.3 at standard establishes a method of communication between PD and PSE consisting of detection, hardware classification, mark events, inrush current limit and normal operation.

The SQ33607 is an integrated PoE solution with IEEE 802.3af/at PD interface and a fully-featured peak current mode Flyback controller.

Detection

In order to identify a device as a valid PD, the PSE senses the Ethernet connection by applying two voltages in the range of 2.8 V to 10.1 V on the Ethernet cable and measuring the corresponding currents. An equivalent resistance is calculated using the ΔV/ΔI. During this phase, the PD must present a resistance between 23.75 kΩ and 26.25 kΩ. A 24.9kΩ (±1%) resistor between VDD and DEN is recommended to present a correct signature.

Classification

In the classification mode, the PSE presents a fixed voltage between 14.5 V and 20.5 V to the PD. The PD controller places a voltage of approximately 2.5 V across the external resistor (R_{CLS} in Fig. 1). The external resistor connected between the CLS pin and VSS provides a classification signature to the PSE. The current drawn by this resistor, combined with the internal current drawn of the controller and any leakage through the internal pass MOSFET, creates the classification current. Table 1 lists the external resistor values required for each of the PD power ranges defined by IEEE802.3at.

The SQ33607 disables classification while the adaptor input is used to avoid excessive power dissipation. If the PD thermal shutdown is triggered or the DEN is active, the CLS reference voltage will be turned off.

Table 1. Class Resistor Selection

Class	Power at PD(W)	Class Current(mA)	Class Resistor(Ω)
0	0.44~12.05	0~4	1270
1	0.44~3.84	9~12	243
2	3.84~6.49	17~20	137
3	6.49~12.95	26~30	90.9
4	12.95~25.5	36~44	63.4

2-Event Classification, Mark Event and T2P Indicator

The SQ33607 can be used as a Type-1 PD class 0-3 (as shown in Table 1). It also can be used as Type-2 PD class 4 with 2-event classification. In 2-event classification, the Type-2 PSE reads the power classification twice. Figure 3 shows an example of a 2-event classification. The first classification event occurs when the PSE presents a voltage between 14.5V to 20.5V to the SQ33607, and the SQ33607 draws a class- 4 load current. The PSE then drops the output voltage to the mark voltage range of 6.9V to 10.1V, signaling the first mark event. The SQ33607 presents a load current between 0.5mA to 2mA for the mark event voltage range. The PSE repeats this sequence, signaling the second classification and second mark event.

The PSE then applies power to the SQ33607, which charges up the DC/DC input capacitor (C_2, C_3 in Fig. 1) with a controlled inrush current. When the DC/DC input capacitor is fully charged and inrush delay finished, T2P presents an active-low signal with respect to RTN to indicate that a Type-2 PSE is available.

When a wall adaptor is detected, the T2P will be pulled low to RTN, too. The T2P is intended to drive the diode side of an optocoupler and should be left open or tied to RTN if not used.

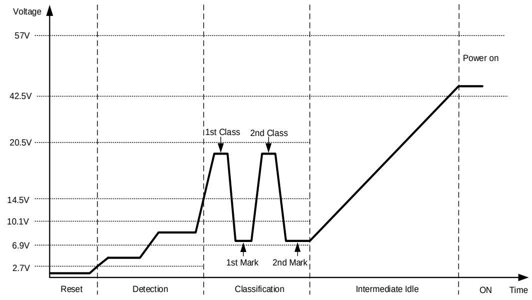


Fig.4 Type-2 PSE, 2-event Classification Sequence

PD Interface UVLO and Current Limit

Once the classification is successfully completed, the PSE will rise its voltage. When the input voltage is above the UVLO turn-on threshold, the hot-swap switch will be turned on, and the input capacitor of the downstream DC/DC converter will be charged with a controlled inrush current. If both of the following conditions are met, which means inrush has been finished, then the current limit will be changed to operating limit and VCC of DC/DC converter will be charged.

1) RTN drops below 1.2V.

2) From VDD>UVLO begins, a 100ms timing named inrush delay is satisfied.

As shown in below figure, there are two sections for the inrush current during inrush interval after VDD>UVLO. When RTN is higher than 20V, the inrush current will be kept around 60mA. As the RTN voltage decreases below 20V, the inrush current will rise to around 100mA until RTN voltage falls below 1.2V and the inrush delay is completed.

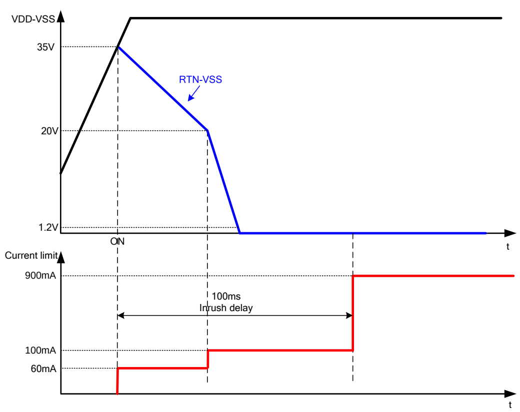


Fig.5 Inrush Current and Inrush Delay

Auto-Maintain Power Signature (A-MPS)

The maintain power signature is an electrical signature presented by the PD to signal the PSE that it is still present after operating voltage is applied. For a Type 1 or Type 2 PD, a valid MPS consists of a minimum dc current of 10mA, or a 10mA pulsed current for at least 75ms every 325ms.

If the current through the RTN-to-VSS path is below 29mA, the SQ33607 will automatically generate a 2.5V maintain power signature pulsed voltage to the AMPS pin, and the current amplitude can be adjusted through an external resistor. When the current through the RTN-to-VSS path is higher than 32mA, the SQ33607 exits maintain power signature mode and clears the maintain power signature flag immediately.
Note that the maintain power signature function is enabled only after the PoE input has been detected.

Adapter Power Input

In some applications, it is desirable to power the PD from an auxiliary power source such as a wall adapter.

The adaptor detection can be enabled if the VDD-RTN voltage exceeds 9V. The voltage divider for adaptor detection is connected as shown in below figure. There is a -1.5V reference for adaptor detection with respect to VDD. When a wall adapter is detected, the internal hot-swap MOSFET between RTN and VSS will be turned off, the classification current will be disabled and the T2P will become active low.

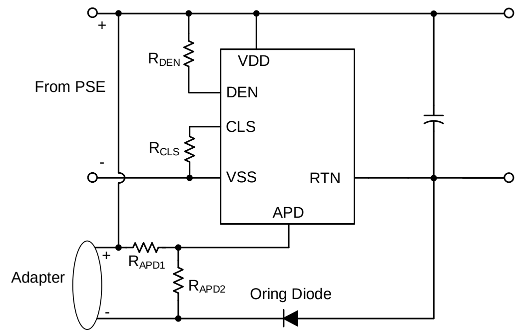


Fig.6 Connection for Adaptor Detection

Hotswap Current Foldback

In order to protect the hotswap MOSFET from damage when OLP, SCP, hot plug or surge events happen, if V_{RTN} rises above 10.5V for longer than 1.1ms during normal operation, the current limit will revert to the inrush value. When the V_{RTN} falls below 1.2V again, the current limit is restored to the operating value.

DC/DC Converter Operation

Start-up Operation

After 100ms inrush delay, the RTN voltage will be almost as low as VSS, the capacitor across VCC and GND pins, C_{VCC} will be charged by the VDD voltage through the internal start-up circuit. Once the VCC voltage reaches V_{VCC_ON}, the start-up charge current will be turned off, and if there is no fault and MODE/FRS pin detection is complete, the DC/DC converter will start operating. The start-up charge current will be turned on again if VCC decreases to V_{VCC_MIN}(~6V) due to the power consumption until the auxiliary winding of Flyback transformer can supply sufficient energy to maintain V_{VCC} above V_{VCC_MIN}.

If faults happen, the PWM switching stops, and the device switches to hiccup mode operation. In this mode, the hiccup off timer (64ms) will start, the start-up charge current will be turned on as needed to maintain the V_{VCC} between 7V and 6V. When the hiccup off time is over, the start-up charge current will be turned off, and when V_{VCC} decreases to 5V, the device enters the re-start sequence.

The device operation is shown in Figure 7.

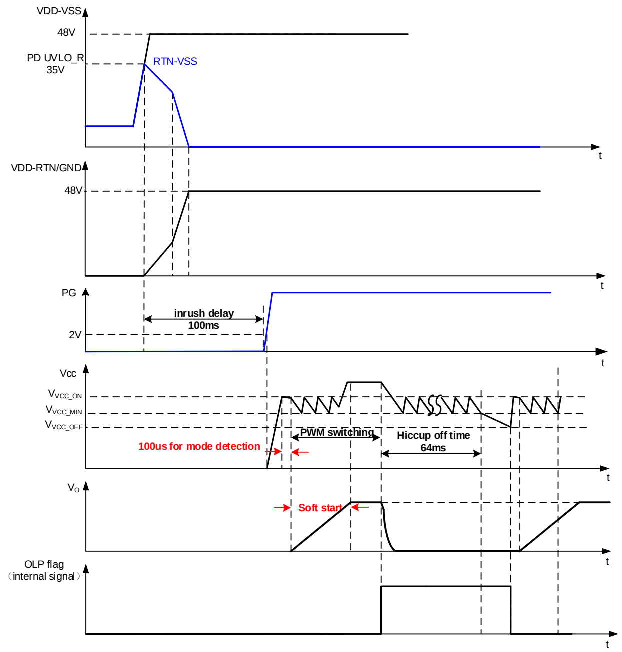


Fig.7 VCC Startup

Operating Mode Detection

After being enabled, the SQ33607 will source a 40μA current to MODE/FRS pin to detect the resistor setting. There are three operating modes which can be selected by setting the resistance value between MODE/FRS pin and GND. Refer to the table below for details.

Table 2. MODE Pin Program Options

MODE/FRS to GND Resistance			Working Mode
Min	Typical	Max	
0	0	1.8kΩ	PSR, 250kHz
7.5kΩ		37.5kΩ	SSR, F_{SW}=3750/R_{mode} (kΩ)
68kΩ	open		PSR, 400kHz

Output Voltage Control in PSR Mode

In order to achieve the primary side constant voltage control, the output voltage is detected by measuring the auxiliary winding voltage using the FB pin during the secondary side output diode conduction period. As shown in Fig.8 and Fig.9, When the secondary-side diode is conducting, the FB voltage can be calculated using equation (1).

$$V_{FB}=V_{AUX}*\frac{R_{FBD}}{R_{FBU}+R_{FBD}}=\left(V_{OUT}+V_{D\_F}\right)*\frac{N_{AUX}}{N_S}*\frac{R_{FBD}}{R_{FBU}+R_{FBD}} \quad (1)$$

Where N_{AUX} is the turns of auxiliary winding; N_S is the turns of secondary winding; V_{D_F} is the forward voltage drop of the secondary-side diode. R_{FBD} and R_{FBU} are part of the the resistor divider used for FB sampling.

Fig.8 shows the FB sample control in discontinuous conduction mode (DCM), Fig.9 shows the FB sample control in continuous conduction mode (CCM).

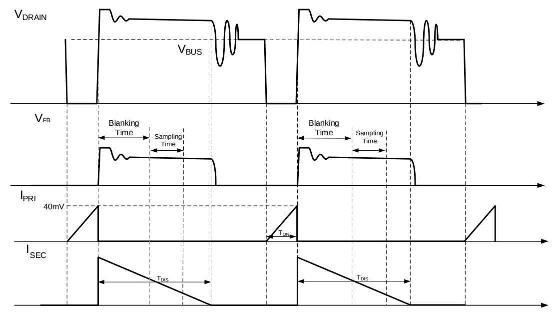


Fig.8 FB Sampling in DCM

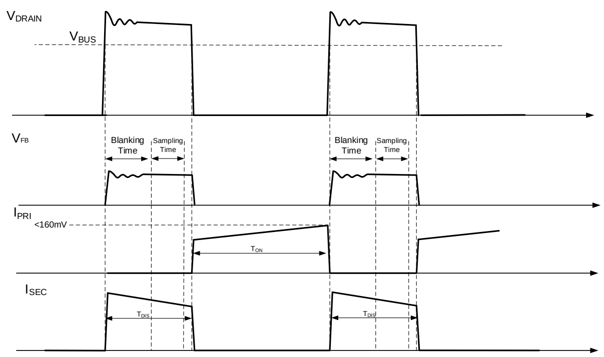


Fig.9 FB Sampling in CCM

The SQ33607 regulates the primary side MOSFET switching to ensure a peak current always ≥V_{CS_MIN}/R_{CS} in PSR mode, and will start sampling the auxiliary-winding voltage after the power MOSFET is turned off. A blanking time is added to avoid measurement during the ringing caused by the leakage inductance. To guarantee long enough FB sample period, the output diode current conduction time （T_{DIS} in Fig8 and Fig.9） should always be longer than 600ns in PSR 400kHz mode, and be longer than 800ns in PSR 250kHz mode.

In SSR mode, FB pin should be connected to GND and the voltage sampling function is disabled.

Output Voltage Compensation in PSR Mode

To get good load regulation in PSR mode, the secondary diode voltage drop and the voltage drop on winding resistance are compensated. A sink current in FB pin which varies as the peak current is usef for compensation during the FB sampling period.

The compensation current can be calculated using the equation (2).

$$I_{FB\_SINK}=5uA*\frac{V_{CS}-40mV}{100mV} \quad (2)$$

In SSR mode, this voltage compensation function is disabled.

Current Sense, Over Current Protection (OCP) and Short Circuit Protection (SCP)

The SQ33607 uses a peak current mode Flyback control loop. The current through the external MOSFET is sensed through a sense resistor that is connected in series with the MOSFET source.

The voltage sensed at the CS/OTP pin during ON time is fed to the high-speed current comparator for current mode control.

If the voltage sensed at the CS/OTP pin is above the V_{CS_MAX}, the comparator will turn off the MOSFET for the current cycle and keep it off until the internal oscillator starts the next cycle and senses the current again, resulting in a cycle-by-cycle current limit.

If the load continues increasing after the OCP protection is triggered, the output voltage will decrease, the COMP voltage will rise, and the peak current will trigger OCP every cycle. The SQ33607 sets the overload detection by continuously monitoring the $V_{CS/OTP}$ voltage. Once the soft-start finishes, the over load protection (OLP) is enabled. If the OCP signal is detected continuously, and lasts more than 4ms, the DC/DC controller turns off the GATE driver and registers the event as overload protection (OLP). After 64ms hiccup off time, the SQ33607 will re-start with a new start-up cycle.

If the peak current cannot be limited by COMP in every cycle due to the minimum gate on time, the current may further increase and transformer may run into saturation. If the monitored V_{CS} voltage reaches 0.25V once, the off time will be forced to max toff, then if V_{CS} reaches 0.25V for the second time, the DC/DC controller registers it as short circuit protection (SCP), it will immediately terminate PWM switching and run into hiccup mode with 64ms hiccup off time, until the condition is removed.

Over Load Protection (OLP) Compensation

The higher input voltage will always lead to higher over-load current limit when the peak current limit is constant, especially in wide input range applications, such as V_{IN}=9V~57V. To solve this problem, an over-load compensation is used as shown in Fig.10.

The over-load compensation current flows out of CS/OTP pin, with a compensation voltage generated across the external compensating resistor R_{OLC}. This is superimposed on the current sensing voltage and the sum is used to drive the input of peak current comparator.

The over-load compensation current is controlled by the internally derived T_{off} duty cycle signal. The control curve is shown in Fig.11. Adjusting the external resistor R_{OLC} enables selecting the proper compensation amplitude.

The over-load compensation is only needed when the current sensing voltage is close to the maximum allowed value. Under the light-load conditions, the compensation current I_{OLC} is disabled.

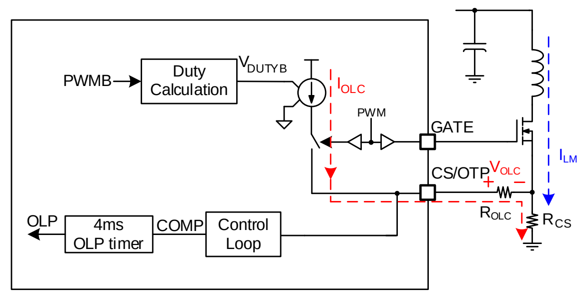


Fig.10 Over Load Compensation

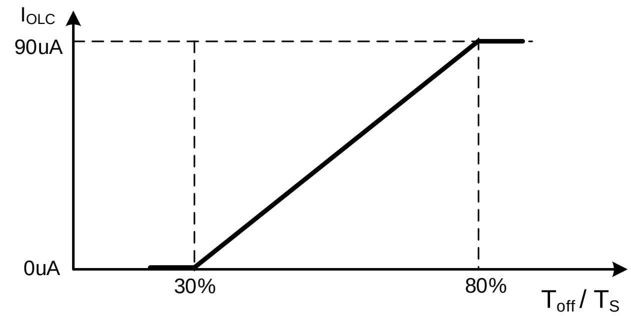


Fig.11 T_{off} Duty Cycle VS. I_{OLC}

Soft Start

The SQ33607 provides a soft-start circuit based on charging an external capacitor with an internally generated constant current. Adjusting the external soft-start capacitor enables adjusting the soft-start time. The soft-start capacitor will be discharged completely when protections are triggered or during thermal shutdown.

The SS signal clamps COMP voltage in SSR mode, and it clamps internal V_{REF} in PSR mode.

Clock Frequency Modulation

The device integrates a spread spectrum clock frequency modulation circuit to minimize EMI emissions. The modulation period is 4ms and the modulation range is ±6% of the switching frequency.

Line Undervoltage Detector

The SQ33607 monitors the line voltage and enables the controller when the input voltage is within the required range. The input voltage is sampled using a resistor divider connected to the UVLO pin. A small decoupling capacitor is recommended for noise filtering.

The controller transitions into the enable mode once V_{UVLO} exceeds V_{enable}. Once in enable mode, the controller is allowed to start if no other faults are present. An internal pull-down current source $I_{UVLO\text{-}hys}$, with a typical value of 20 μA provides hysteresis.

$I_{UVLO\text{-}hys}$ turns off once the controller is enabled, allowing V_{UVLO} to rise above V_{enable} by the hysteresis level set by R_{UV1}. The controller is disabled if V_{UVLO} falls below V_{UVP}, at which point $I_{UVLO\text{-}hys}$ is re-enabled creating a voltage drop on the UVLO pin.

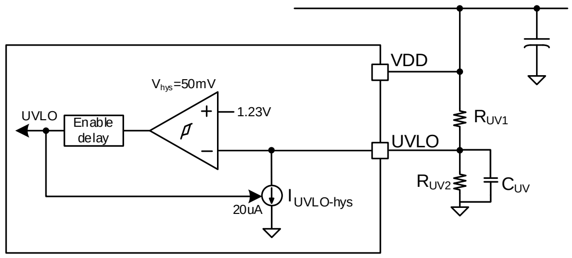


Fig.12 UVLO Block Diagram

Output Over Voltage Protection in PSR Mode

In PSR mode, if the sampled voltage at FB pin exceeds 120% of V_{REF} for 4 consecutive switching cycles, which means OVP condition has been occurred, the device stops switching and enters hiccup mode immediately. After the 64ms hiccup off time, the device will attempt to restart. It returns to normal operation as soon as the condition disappears.

External OTP

If temperature monitoring of the external MOSFET or transformer is needed, an external NTC resistor placed close to the component can be used. The NTC resistor forms a voltage divider with R_{OLC}+R_{CS} during secondary diode conduction period, as shown in fig.13. When the temperature increases, the NTC resistance becomes lower and the CS/OTP pin voltage increases.

When the detected voltage exceeds 1V for 4 consecutive cycles, the device register the event as an external OTP. The switching stops immediately and the device enters hiccup mode. When the detected voltage falls below 0.92V, the device resumes normal operation.

A resistor R_{adj} connected in series with NTC can be used to adjust the divider ratio and therefore adjust the OTP threshold.

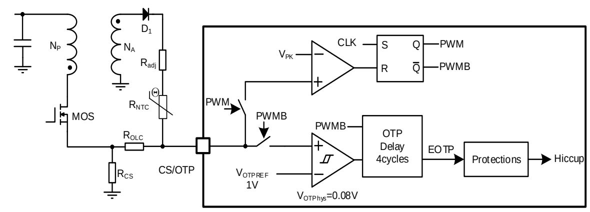


Fig.13 External OTP

VCC Over Voltage Protection

When the VCC voltage exceeds the V_{VCC_OVP} threshold, the device stops switching enter hiccup mode. After 64ms hiccup off time ends, the device will restart. It will continues to operate in this mode until the overvoltage condition disappears.

Typical Application Schematic

In this design, the PSE or 42.5VDC~57VDC can be accepted as power supply, the converter is designed to deliver 12V and 2.1A.

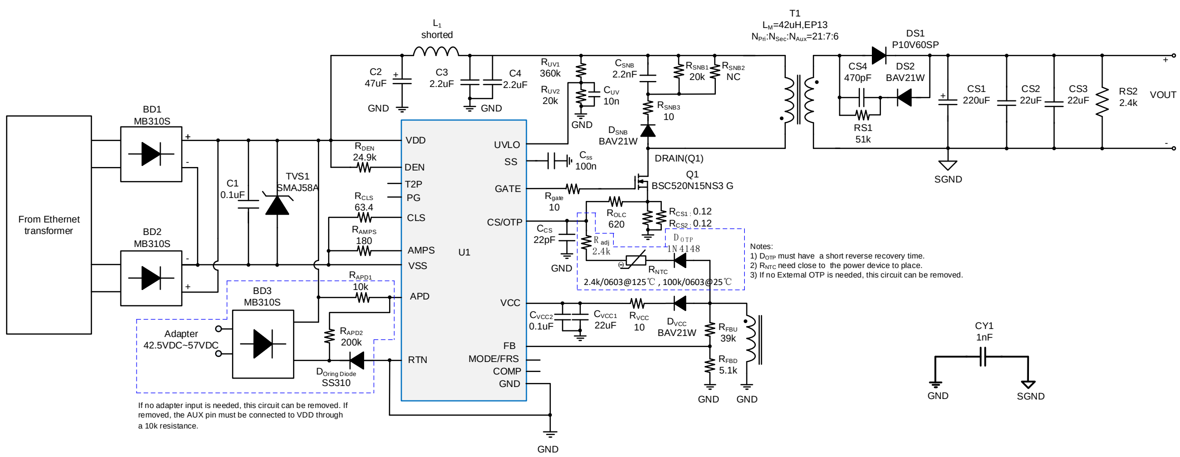


Figure 14. Typical Application-Isolated PSR Flyback Converter

Recommended BOM List

Designator	Description	Part Number	Manufacturer
C1	0.1uF/100V,X7R,±10%,0805	AC0603KRX7R0BB104	YAGEO
C2	47uF/63V, Aluminium Electrolytic Capacitors ,D8xL12mm	ERF1JM470F12C30T	AISHI
C3	2.2uF/100V, Ceramic capacitor,X7R,±10%,1206	CC1206KKX7R0BB225	YAGEO
C4	2.2uF/100V, Ceramic capacitor,X7R,±10%,1206	CC1206KKX7R0BB225	YAGEO
C_{UV}	10nF/25V, Ceramic capacitor, X7R,±10%,0603	CC0603KRX7R8BB103	YAGEO
C_{SNB}	2.2nF/250V, Ceramic capacitor, X7R,±10%,0805	CC0805JKNPOYBN222	YAGEO
C_{ss}	100nF/25V, Ceramic capacitor, X7R,±10%,0603	CC0603KRX7R8BB104	YAGEO
C_{CS}	22pF/25V, Ceramic capacitor, NPO,±5%,0603	CC0603JRNPO8BN220	YAGEO
C_{VCC2}	0.1uF/25V, Ceramic capacitor, X7R,±10%,0603	CC0603KRX7R8BB104	YAGEO
C_{VCC1}	22uF/25V, Ceramic capacitor, X7R,±10%,0805	CC0805MFX7R8BB226	YAGEO
CS1	220uF/16V, Aluminium Electrolytic Capacitors(Solid state capacitance), D6.3xL8mm,	SPZ1CM221E08O00RAXXX	AISHI
CS2	22uF/25V, Ceramic capacitor, X5R,±20%,1206	CC1206MKX5R8BB226	YAGEO
CS3	22uF/25V, Ceramic capacitor, X5R,±20%,1206	CC1206MKX5R8BB226	YAGEO
CS4	470pF Ceramic capacitor, X7R,±10%,0805	CC0805KRX7R0BB471	YAGEO
CY1	1nF/ 2kV, Ceramic capacitor, X7R,±10%,1206	CC1206KKX7RDBB102	YAGEO
BD1,BD2,BD3	3A/100V,Schottky bridge, MBS Package	MB310S	Jingdao
TVS1	TVS diode,SMA	SMAJ58A	Jingdao
$D_{Oring\ Diode}$	3A/100V,Schottky Diode, SMA	SS310	Jingdao
D_{SNB}	250V/250mA,Diode,SOD-123	BAV21W	Jingdao
D_{VCC}	250V/250mA,Diode,SOD-123	BAV21W	Jingdao
Q1	150V/52mΩ/ 21A, NMOS,PG-TDSON-8	BSC520N15NS3 G	Infineon
DS1	10A/60V,Schottky Diode, TO-277	P10V60SP	PFC Device
DS2	250V/250mA,Diode,SOD-123	BAV21W	Jingdao
R_{DEN}	24.9k, ±1%,0603	RC0603FR-0724K9L	YAGEO
R_{CLS}	63.4, ±1%,0603	AC0603FR-0763R4L	YAGEO
R_{AMPS}	180, ±1%,0603	RC0603FR-07180RL	YAGEO
R_{APD1}	10k, ±5%,0603	RC0603JR-0710KL	YAGEO
R_{APD2}	200k, ±1%,0603	RC0603FR-07200KL	YAGEO
R_{UV1}	360k, ±1%,0603	RC0603FR-07360KL	YAGEO
R_{UV2}	20k, ±1%,0603	RC0603FR-0720KL	YAGEO
R_{SNB1}	20k, ±1%,0805	RT0805BRD0720KL	YAGEO
R_{SNB2}	NC	/	/

R_{SNB3}	10, ±1%,0805	RC0805FR-0710RL	YAGEO
R_{gate}	10, ±1%,0805	RC0805FR-0710RL	YAGEO
R_{OLC}	620, ±1%,0603	RC0603FR-07620RL	YAGEO
R_{CS1}	0.12, ±1%,1206	RL1206FR-7W0R12L	YAGEO
R_{CS2}	0.12, ±1%,1206	RL1206FR-7W0R12L	YAGEO
R_{adj}	2.4k, ±1%,0603	RC0603FR-072K4L	YAGEO
R_{NTC}	NTC Thermistor,0603 (2.4k/0603@125℃ ,100k/0603@25℃)	DNT1608X104□3950◎TF	Sunlord
R_{VCC}	10, ±1%,0603	RT0603BRD0710KL	YAGEO
R_{FBU}	39k, ±1%,0603	RC0603FR-0739KL	YAGEO
R_{FBD}	5.1k, ±1%,0603	RC0603FR-075K1L	YAGEO
RS1	51k, ±1%,1206	RC1206FR-0751KL	YAGEO
RS2	2.4k, ±1%,1206	RC1206FR-072K4L	YAGEO
L_1	shorted	/	/
T1	L_M=42uH,EP13 N_{Pri}:N_{Sec}:N_{Aux}=21:7:6	750345603	Wurth Elektronik
U1	IEEE 802.3af/at Compliant PoE PD Interface with high Efficiency PSR/SSR Flyback Controller	SQ33607QYQ	SILIERGY

Design Procedure and Example

A step by step design example of a typical PSR application is shown below:

Design Note:
1. In all operating conditions, the secondary diode conduction time should be longer than 600ns (400kHz PSR)/800ns (250kHz PSR) for sufficient sampling time.
2. R_{FBU} is the upper resistor of the divider, and has a recommended value between 18kΩ~51kΩ.

Design Specifications

Design Specifications			
V_{IN}	42.5V~57V	η	88%
V_{OUT}	12V	I_{OUT}	2.1A

PD Input Capacitor Setting

Select the detection and classification resistors as outlined in the datasheet (pinout table and table1). In addition, a 0.05μF to 0.12μF input capacitor (C1 in Fig.15) is required to meet IEEE 802.3at/af standard specifications. It is recommended to use 68nF, 82nF or 100nF, 100V ceramic capacitor.

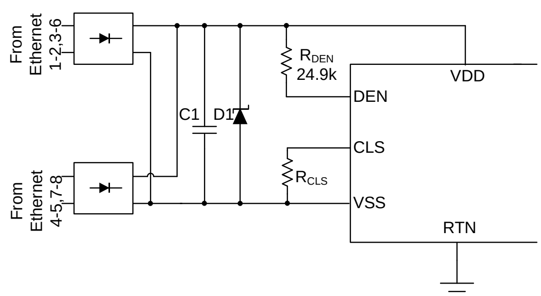


Fig.15 PD Input Connection

Protection TVS Setting

To limit the input transient voltage to a value below the absolute maximum ratings of SQ33607, a transient voltage suppressor (TVS) diode (D1 in Fig.15) must be placed across the rectified voltage (VDD - VSS). An SMAJ58A (or equivalent) diode is recommended for general indoor applications. Outdoor transient levels or special applications require additional protection.

Transformer N_{PS} and L_M Selection

N_{PS} is limited by the breakdown voltage of the power MOSFET:

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - V_{DC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (3)$$

Where $V_{MOS\_(BR)DS}$ is the breakdown voltage of the power MOSFET.

In constant frequency, continuous conduction mode, each switching period cycle t_S consists of two parts: current rising time T_{ON}, current falling time T_{DIS}, as shown in Fig.9.

For a selected turns ratio, the duty cycle can be calculated with equation (4)

$$\text{Duty Cycle}=\frac{N_{PS}*V_{OUT}}{V_{IN}+N_{PS}*V_{OUT}} \quad (4)$$

The maximum duty cycle means minimum T_{DIS}, so the duty cycle at the lowest input voltage should be checked to ensure long enough sampling time.

The primary-side inductance affects the input current ripple factor. A high inductance results in a large transformer size and high cost; a low inductance results in high switching peak current and RMS current, which causes a decrease in efficiency. Choose a primary-side inductance to make the current ripple ratio factor around 30% ~ 50%. Estimate the primary-side inductance with:

$$L_M=\frac{(V_{IN}*D)^2}{2*f_{sw}*P_{IN}*k_{RF}} \quad (5)$$

Where k_{RF} is the current ripple factor, P_{IN} is the input power, and L_M is the primary inductance.

Calculate L_M based on the minimum input voltage condition.

The leakage inductance leads to power loss and voltage stress on the MOSFET. Normally, the leakage inductance should be controlled to be below 3% of the transformer inductance.

Once the CCM frequency f_{SW} and K_{RP} is set, the inductance of the transformer can be calculated:

(a) Compute turns ratio N_{PS} first

$$N_{PS}\le\frac{V_{MOS\_(BR)DS}\times 90\%-V_{DC\_MAX}-\Delta V_S}{V_{OUT}+V_{D\_F}}=\frac{150*0.9-57-30}{12.5}=3.84$$

N_{PS} is set to

$$N_{PS}=3$$

(b) Compute maximum duty cycle and check the min T_{DIS} in heavy load (frequency accuracy and jitter need to be considered)

$$D_{MAX}=\frac{N_{PS}*(V_{OUT}+V_{D\_F})}{V_{IN\_MIN}+N_{PS}*(V_{OUT}+V_{D\_F})}=\frac{3*(12+0.5)}{42.5+3*(12+0.5)}=0.469$$

$$T_{DIS\_MIN}=(1-D_{MAX})*T_{SW}=(1-0.469)*2.5us*90\%*94\%$$

$$=1.123us>600ns$$

(c) Compute inductor L_M

$$L_M=\frac{(V_{IN\_MIN}*D_{MAX})^2}{2*f_{sw}*P_{IN}*k_{RF}}=\frac{(42.5*0.469)^2}{2*400k*\frac{25.2}{0.88}*0.4}=43.31uH$$

Select: L_M=42.0μH

MOSFET and DIODE Setting

The minimum voltage rating of the MOSFET and power diode are calculated at the maximum input voltage and full load.

$$V_{MOS\_DS\_MAX}=V_{DC\_MAX}+N_{PS}\times(V_{OUT}+V_{D\_F})+\Delta V_S \quad (6)$$

$$V_{D\_R\_MAX}=\frac{V_{DC\_MAX}}{N_{PS}}+V_{OUT} \quad (7)$$

Where V_{DC_MAX} is maximum input DC voltage; N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the rated output voltage; V_{D_F} is the forward voltage of secondary power diode; ΔV_S is the overshoot voltage clamped by RCD snubber during OFF time.

The minimum current rating of the MOSFET and power diode are calculated using minimum input voltage and full load:

$$I_{MOS\_PK\_MAX}=I_{P\_PK\_MAX} \quad (8)$$

$$I_{MOS\_RMS\_MAX}=I_{P\_RMS\_MAX} \quad (9)$$

$$I_{D\_PK\_MAX}=N_{PS}\times I_{P\_PK\_MAX} \quad (10)$$

$$I_{D\_AVG}=I_{OUT} \quad (11)$$

Where $I_{P\_PK\_MAX}$ and $I_{P\_RMS\_MAX}$ are maximum primary peak current and RMS current, which will be introduced later.

After setting the turns ratio and transformer inductance, the current rating of the MOSFET, diode and transformer winding can be calculated as shown below:

Conditions			
V_{IN_MIN}	42.5V	V_{IN_MAX}	57V
ΔV_S	30V	$V_{MOS\text{-}(BR)DS}$	150V
P_{OUT} (max)	25.2W	V_{D_F}	0.5V
Ripple factor	0.4	f_{SW}	400kHz

$$I_{MOS\_PK\_MAX}=I_{P\_PK\_MAX}=\frac{\frac{P_{IN}}{V_{INMIN}}}{Duty}*(1+k_{RF}) \quad (12)$$

$$I_{MOS\_RMS\_MAX}=I_{P\_RMS\_MAX}=\sqrt{\frac{\int_0^{D*Ts}\left[\frac{\frac{P_{IN}}{V_{INMIN}}}{D}(1-k_{RF})+\frac{V_{INMIN}}{L_M}*t\right]^2 dt}{Ts}} \quad (13)$$

$$I_{D\_PK\_MAX}=I_{S\_PK\_MAX}=N_{PS}\times I_{P\_PK\_MAX} \quad (14)$$

$$I_{D\_PK\_MAX}=I_{S\_RMS\_MAX}=\sqrt{\frac{\int_{D*Ts}^{Ts}\left[\frac{N_{PS}*P_{IN}}{V_{INMIN}*D}(1+k_{RF})-\frac{V_{OUT}}{L_M/N_{PS}^2}*(t-D*Ts)\right]^2dt}{Ts}} \quad (15)$$

The design flow is shown below:

(d) Compute maximum primary peak current $I_{P\_PK\_MAX}$, primary RMS current $I_{P\_RMS\_MAX}$, , secondary peak current $I_{S\_PK\_MAX}$, secondary RMS current $I_{S\_RMS\_MAX}$.

$$I_{P\_PK\_MAX}=\frac{\frac{P_{IN}}{V_{IN\_MIN}}}{D_{MAX}}*(1+k_{RF})=\frac{\frac{25.2}{42.5*0.88}}{0.469}(1+0.4)=2.03A$$

$$I_{P\_RMS\_MAX}=\sqrt{\frac{\int_0^{D_{MAX}*Ts}\left[\frac{\frac{P_{IN}}{V_{IN\_MIN}}}{D_{MAX}}(1-k_{RF})+\frac{V_{IN\_MIN}}{L_M}*t\right]^2dt}{Ts}}$$

$$=\sqrt{\frac{\int_0^{1.1725u}\left[0.862+\frac{42.5}{42\mu}*t\right]^2dt}{2.5\mu}}$$

$$=1.023A$$

$$I_{S\_PK\_MAX}=N_{PS}\times I_{P\_PK\_MAX}=3*2.03=6.09A$$

$$I_{S\_RMS\_MAX}=\sqrt{\frac{\int_{D_{MAX}*Ts}^{Ts}\left[N_{PS}*I_{P\_PK\_MAX}-\frac{V_{OUT}}{L_M/N_{PS}^2}*(t-D_{MAX}*Ts)\right]^2dt}{Ts}}$$

$$=\sqrt{\frac{\int_{1.1725u}^{2.5u}\left[6.09-\frac{12}{4.67u}*(t-1.1725u)\right]^2dt}{2.5\mu}}$$

$$=2.977A$$

(e) Select secondary power diode

Refer to Power Device Design

Known conditions:			
V_{DC_MAX}	57V	N_{PS}	3
V_{OUT}	12V	V_{D_F}	0.5V

Compute the voltage and the minimum current rating of the secondary power diode

$$V_{D\_R\_MAX}=\frac{V_{DC\_MAX}}{N_{PS}}+V_{OUT}+\triangle V_S$$

$$=\frac{57V}{3}+12V+15V$$

$$=46V$$

$$I_{D\_PK\_MAX}=N_{PS}*I_{P\_PK\_MAX}=2.03*3=6.09A$$

$$I_{D\_PK\_MAX}=I_{S\_RMS\_MAX}=2.977A$$

Select:

Secondary power diode:10A/60V,Schottky Diode.

Current Sense Resistor Selection

The current sense resistor can be used to limit the switching peak current. The current sense voltage at full load should be around 80% of the V_{CS_MAX}, so the resistance can be calculated with:

$$R_{CS}=\frac{0.8*V_{CS\_MAX}}{I_{P\_PK\_MAX}} \quad (16)$$

(f) Compute the current sense resistor value

$$R_{CS}=\frac{0.8*V_{CS\_MAX}}{I_{P\_PK\_MAX}}=\frac{0.8*0.16}{2.03}=0.063\Omega$$

Select:

R_{CS}=60mΩ

Check the T_{DIS} in no load:

$$T_{DIS\_MIN}=\frac{V_{CS\_MIN}*0.90*L_M*0.95}{R_{CS}*1.01*N_{PS}*(V_{OUT}+V_{D\_F})}=632ns>600ns$$

RCD Snubber for MOSFET

The power stored in the leakage inductance is evaluated first:

$$P_{LK}=0.5*L_{LK}*I_{P\_PK\_MAX}^2\times F_{sw} \quad (17)$$

Where L_{LK} is the leakage inductance of the flyback transformer; I_{P_PK} is the peak current of primary side.

The power of the leakage inductance is dissipated by the resistor R_{RCD}:

$$R_{RCD}=\frac{\left[N_{PS}\times(V_{OUT}+V_{D\_F})+\Delta V_S\right]^2}{P_{LK}} \quad (18)$$

Where N_{PS} is the turns ratio of the flyback transformer; V_{OUT} is the output voltage; V_{D_F} is the forward voltage of the power diode; ΔV_S is the overshoot voltage clamped by RCD snubber;

The C_{RCD} is related to the voltage ripple of the snubber ΔV_{C_RCD}.

$$C_{RCD}=\frac{N_{PS}\times(V_{OUT}+V_{D\_F})+\Delta V_S}{R_{RCD}\times f_S\times\Delta V_{C\_RCD}} \quad (19)$$

(g) Select the RCD snubber.

Suppose the leakage inductance is 1% of the primary inductance.

$$V_{RCD}=N_{PS}*(V_{OUT}+V_{D\_F})+\Delta Vs=57.5V$$

$$P_{RCD}=0.5*42u*0.01*2.03^2*400k=0.346W$$

$$R_{RCD}=\frac{57.5^2}{0.346}=9.55k\Omega$$

Select two 20kΩ resistors in parallel for R_{RCD}.

$$C_{RCD}=\frac{N_{PS}*(V_{OUT}+V_{D\_F})+\Delta V_S}{R_{RCD}*f_S*\Delta V_{C\_RCD}}=\frac{57.5V}{20k*400k*0.3*20V}\approx 2.2nF$$

Transformer Turns Calculation

The key transformer parameters are shown below:

Necessary parameters	
Primary to Secondary Turns ratio	N_{PS}
Inductance	L_M
Primary maximum current	$I_{P\_PK\_MAX}$
Primary maximum RMS current	$I_{P\_RMS\_MAX}$
Secondary maximum RMS current	$I_{S\_RMS\_MAX}$

The design rules are as followed:

(S1) Select the magnetic core style, identify the effective cross-sectional area A_e. EP13 was selected for this example. Its A_e is 19.50 mm². The EP13 can be replaced by other reasonable magnetic core style.

(S2) Preset the maximum magnetic flux density ΔB is 0.26T at minimum BUS voltage and full load.
Usually ΔB=0.2T~0.3T ,set ΔB=0.2

(S3) Compute primary turn N_P

$$N_P=\frac{L_M\cdot I_{P\_PK\_MAX}}{\Delta B\cdot A_e}=\frac{42uH\times 2.03}{0.20T\times 19.50mm^2}=21.86$$

N_P is set to 21
Where A_e is effective cross-sectional area of core

(S4) Compute secondary turn N_S

$$N_S=\frac{N_P}{N_{PS}}=\frac{21}{3}=7$$

N_S is set to 7

(S5) Compute auxiliary turn N_{AUX}
Generally, minimum VCC pin voltage should be guaranteed to be above VCC_MIN，so set VCC=10V. Turns of the auxiliary winding can be initially calculated as shown below:

$$N_{AUX}=N_S\cdot\frac{V_{VCC}}{V_{OUT}}=7\times\frac{10}{12}=5.83$$

N_{AUX} is set to 6

(S6) Select an appropriate wire diameter

With $I_{P\_RMS\_MAX}$ and $I_{S\_RMS\_MAX}$, select appropriate wire to achieve a current density from 4A/mm² to 10A/mm².

Primary wire diameter selection: current density j is set to 12A/mm². Compute primary wire cross-sectional area:

$$S_{Pri}=\frac{I_{P\_RMS\_MAX}}{j}=\frac{1.023}{10}=0.1023mm^2$$

Select wire diameter D1=0.15mm
Number of wires to be parelleled,

$$N_{P\_wire}'=\frac{S_{Pri}}{\pi*(\frac{D1}{2})^2}=\frac{0.1023}{\pi*(\frac{D1}{2})^2}=5.79$$

Set N_{P_wire}=6

Secondary wire diameter selection: current density j is set to 12A/mm². Compute secondary wire cross-sectional area:

$$S_{SEC}=\frac{I_{S\_RMS\_MAX}}{j}=\frac{2.977}{12}=0.2481mm^2$$

Select wire diameter D2=0.20mm
Number of wire to be parelleled,

$$N_{S\_wire}'=\frac{S_{SEC}}{\pi*(\frac{D2}{2})^2}=\frac{0.2481}{\pi*(\frac{D2}{2})^2}=7.90$$

Set N_{S_wire}=8

Consider transformer style, the actual primary and secondary wire diameters can be adjusted for best manufacturability.

(S7) If the window area of the core and bobbin is not enough, reselect the core style, go to (S1) and redesign the transformer until an optimal design of the transformer is achieved.

(S8) The transformer final parameters are shown below

Item	Specification	Remark
EP13 (42.5VDC~57VDC, 25.2W)		
Primary-Side Inductance	42uH±5%	40kHz,1V,25±5 ℃,Hum:65±25%
Primary-Side Leakage Inductance	1.20µH Maximum	Short One of Secondary Winding
N_P	21(0.15mm*6)	
N_S	7(0.20mm*8)	
N_A	6(0.15mm*1)	

Set MODE/FRS pin

Let MODE/FRS pin float to set 400kHz PSR mode operation.

Set FB pin

Refer to Output Voltage Control in PSR Mode part.

Available from the previous design: N_S=7,N_{AUX}=6

First identify R_{FBU} needed for line regulation.

Parameters Designed			
R_{FBU}	39kΩ		

Then compute R_{FBD}

Conditions			
V_{OUT}	12V	V_{FB_REF}	1.2V
R_{FBU}	39kΩ		

$$R_{FBD}=\frac{R_{FBU}}{\frac{V_{OUT}*N_{AUX}}{V_{FB\_REF}*N_S}-1}=\frac{39k}{\frac{12V}{1.2V}*\frac{6}{7}-1}\approx 5.1k$$

Set APD pin

The minimum adaptor input voltage is 37V (V_{IN_MIN}=42.5VDC). Select the a value of 200k for the APD lower resistor R_{APD_D}. The upper resistor can be calculataed using:

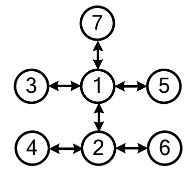
$$R_{APD\_U}=\frac{R_{APD\_D}*1.7}{37V-1.7V}\approx 10k\Omega$$

Layout

(a) To achieve better EMI performance and reduce the line frequency ripple, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

(b) The circuit loop of all switching loops should be kept small: primary power loop, secondary loop and auxiliary power loop.

(c) The connection of primary ground is recommended as shown below:



Ground ①: ground of BUS capacitor.

Ground ②: ground of bias supply capacitor.

Ground ③: ground node of auxiliary winding.

Ground ④: ground node of resistor divider.

Ground ⑤: primary ground node of Y capacitor.

Ground ⑥: device GND.

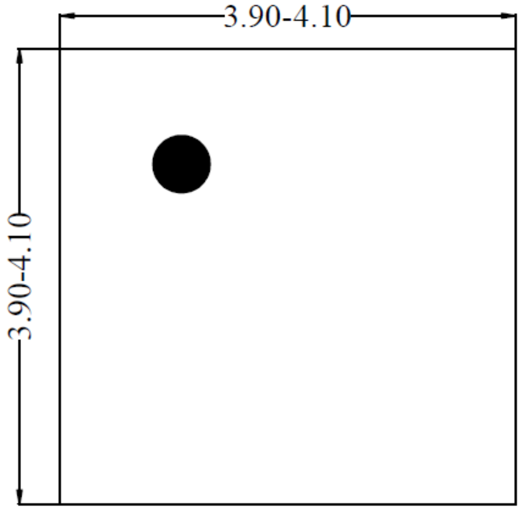
Ground ⑦: ground of current sense resistor.

(d) Bias supply trace should be connected to the bias supply capacitor first instead of GND pin. The bias supply capacitor should be placed near the IC.

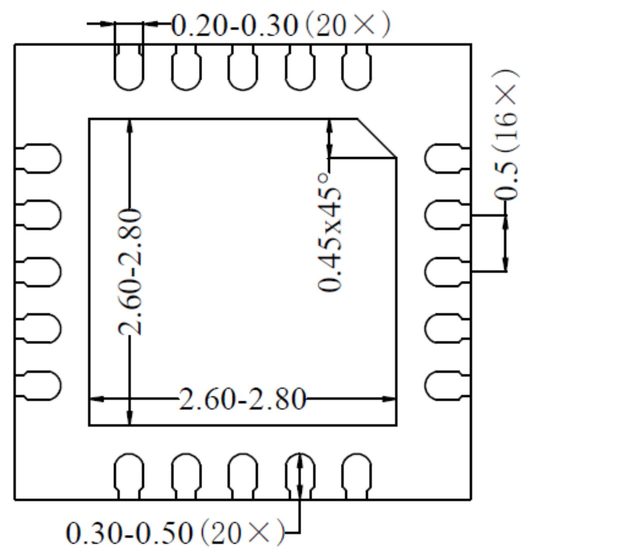
(e) Place the FB resistor divider near the the IC.

(f) The trace spacing between AMPS (low voltage pin) and adjacent pins (high voltage pin) shouldn't be less than the pitch. The same rule applies to the CLS pin.

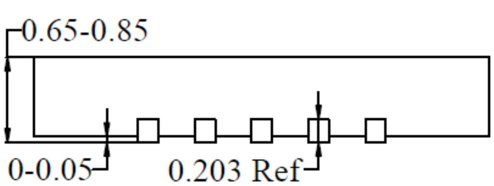
QFN4x4-20 Package Outline Drawing



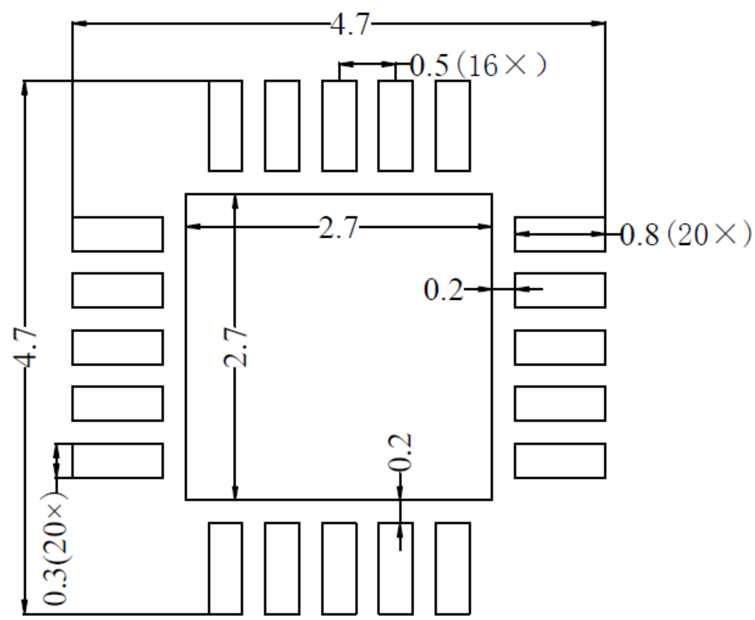
Top View



Bottom View



Front View

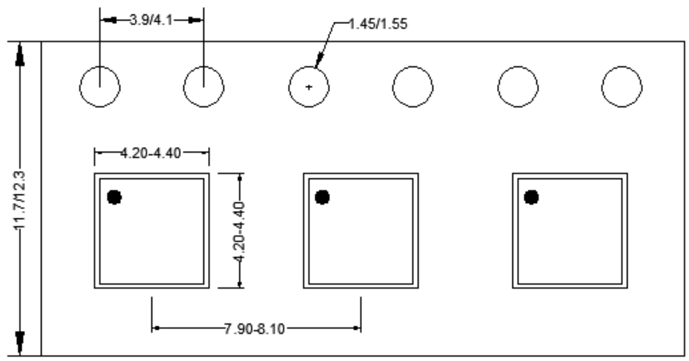


Recommended PCB layout (Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

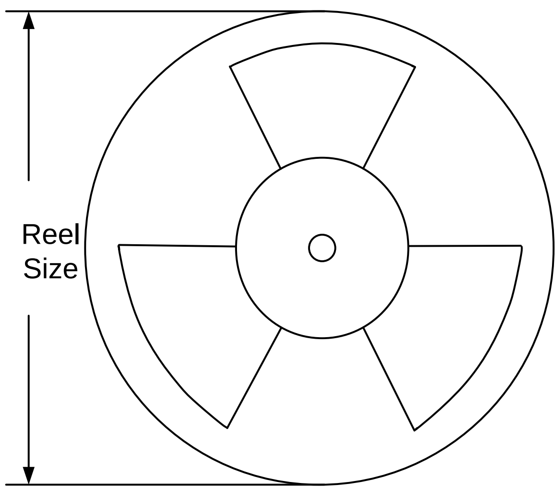
Tape and Reel Specification

1. QFN4×4 Taping Orientation



Feeding direction

2. Carrier Tape and Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
QFN4x4	12	8	13"	400	400	5000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
April 26, 2024	Revision 1.0	Initial Release

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